

Figure 1:
Block diagram of the Cortex-R82 processor

Overview

The Cortex-R82 processor is the first Armv8-R 64-bit processor and enables the higher compute performance needed for the next generation of data storage and to run new workloads, such as machine learning (ML). It is Arm's first Cortex-R processor to support a trusted and robust ecosystem of rich operating systems and software components that already exist in the Linux and cloud development ecosystem.

Features

Feature	Description
Architecture	Armv8-R, AArch64 architecture, A64 instruction set. Compliant with Armv8.4-A extensions.
Pipeline	Eight-stage, in-order, superscalar pipeline with direct and indirect branch prediction.
Bus Architecture	AMBA 5 AXI and ACE protocol. AMBA 4 AXI4-Stream protocol for interrupts. AMBA 4 APB protocol for debug. AMBA 4 ATB protocol for debug. AMBA CHI protocol.
Security	Secure state operation only at all Exception levels (EL0 to EL2). Compatible with Arm TrustZone technology.
Cache Protection	Reliability, Availability, and Serviceability (RAS) Extension. Optional Error Correcting Code (ECC), Single Error Correct Double Error Detect (SECEDED) or Double Error Detect (DED) protection for all of the instantiated caches, cache tag and data RAMs and the TCM RAMs.
Generic Interrupt Controller (GIC)	GIC CPU interface to connect to an external GICv3.2 interrupt distributor.
Generic Timer	Generic Timer interface supporting 64-bit count input from an external system counter.
Floating Point	Optional Half Precision (HP), Single Precision (SP) and Double Precision (DP) floating-point architecture support, and Advanced Single Instruction Multiple Data (SIMD), also known as Neon technology.
L1 Cache	Separate L1 data cache and L1 instruction cache private to each core.
L2 Cache	An optional, shared (between all cores), and unified (instructions and data) L2 cache. Partial L2 cache power-down support.

Tightly Coupled Memories (TCMs)	Two optional TCMs private to each core: an ITCM for instructions and literal pool data and a DTCM for data.
Debug	Armv8-R AArch64 debug logic with debug over power-down support.
	Cross Trigger Interface (CTI) for multiprocessor debugging.
	Optional support for integrating CoreSight Embedded Logic Analyzer, ELA-600 for advanced debug capability and signal observability.
	Performance Monitors Extension support for software profiling and performance debugging based on the PMUv3 architecture.
	Memory Built-In Self-Test (MBIST) for testing memories at boot time.
Trace	Embedded Trace Macrocell (ETM), compliant with ETMv4.5, for instruction and data trace.
Memory Protection Unit (MPU)	Two programmable MPUs controlled from EL1 and EL2 respectively, for determining the attributes for each memory location including permissions, type, and cacheability.
Memory Management Unit (MMU)	Fine-grained memory system control through virtual-to-physical address mappings and memory attributes held in translation tables.

About the Cortex-R82 Processor

The Cortex-R82 processor is a high-performance, high-efficiency, multi-core, in-order, superscalar processor for use in real-time embedded applications. The Cortex-R82 processor implements the Armv8-R AArch64 architecture.

Interfaces supported by the processor include:

- + AMBA 5 AXI
- + AMBA 4 AXI4-Stream
- + AMBA 4 APB
- + AMBA 4 ATB
- + AMBA CHI
- + Instruction ATB trace
- + Data ATB trace
- + AMBA ACE5-Lite
- + Q-channel
- + P-channel
- + CTI

About the Cortex-R82 Processor

The processor has optional:

- + Tightly Coupled Memories (TCMs) that are private to each core, an ITCM for instructions and literal pool data and a DTCM for data.
- + Shared (between all cores), and unified (instructions and data) L2 cache.
- + Shared AXI5 256-bit Low-latency RAM (LLRAM) port for instruction and data access.
- + Shared AXI5 64-bit Shared Peripheral Port (SPP) for peripheral access.
- + Per-core AXI5 32-bit Low-latency Peripheral Port (LLPP) for peripheral access.
- + Error Correcting Code (ECC), Single Error Correct Double Error Detect (SECCDED) or Double Error Detect (DED) protection for all instantiated cache tag and data RAMs and the TCM RAMs.
- + Support for integrating CoreSight Embedded Logic Analyzer, ELA-600 for advanced debug capability and signal observability.

Block Diagram

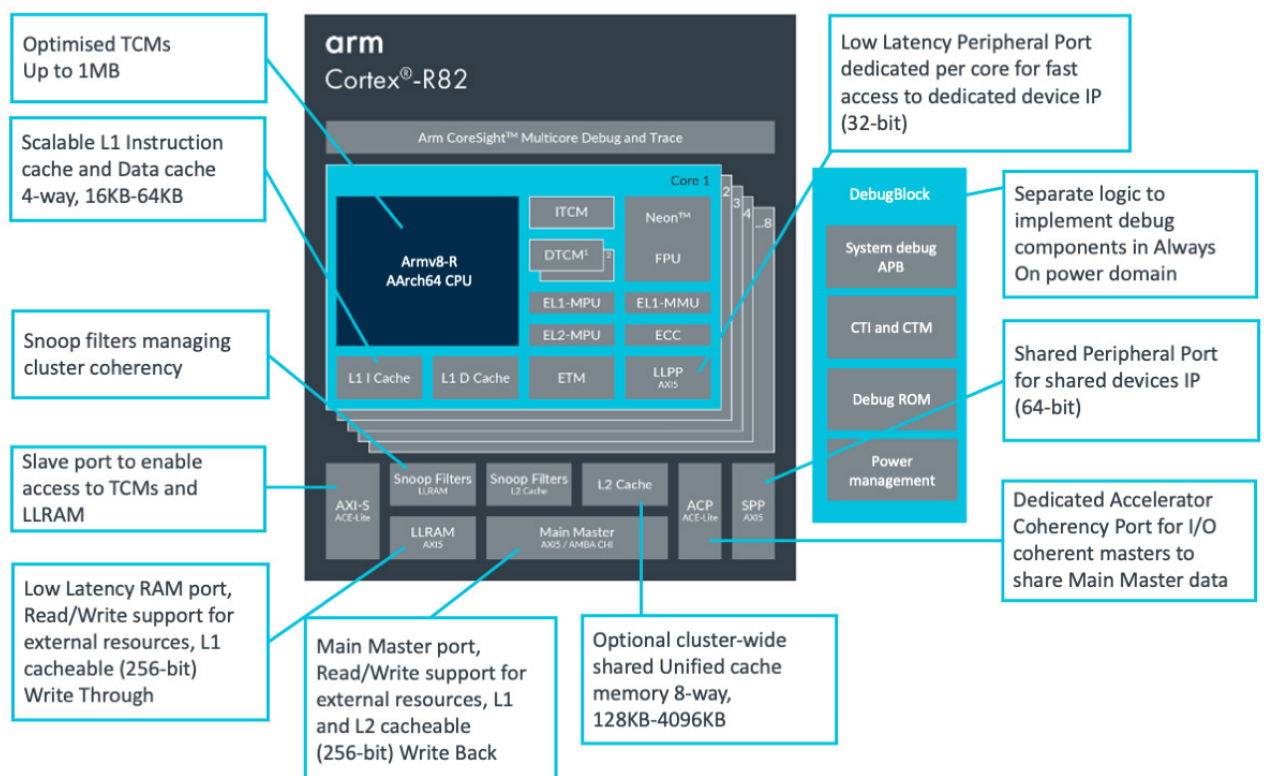


Figure 2: Cortex-R82 processor components

Cortex-R82 Components

The Cortex-R82 processor system includes two top-level modules:

- + The Cortex-R82 processor
- + The DebugBlock

The DebugBlock is separated from the Cortex-R82 processor to allow the implementation of the debug components in an always-on power domain, enabling debug over power-down.

Power Policy Units

The Cortex-R82 processor includes one Power Policy Unit (PPU) per core and one PPU for the processor cluster that control power modes and resets. The PPUs can be programmed to directly select a specific power mode or to autonomously switch between power modes within a specified range, based on the requirements of the processor. The PPUs can be programmed using the Utility bus, either by a System Control Processor (SCP) or by the Cortex-R82 processor (through a loopback connection).

Shared Bridge

The Shared Bridge (SB) decouples the DebugBlock and other components in the system from the CPU bridge in each core. The SB includes clock and power control logic for the cluster and interacts with the L2 coherency logic for SCLK clock gating.

L2 coherency logic

The L2 coherency logic maintains coherency between all the cores and caches within the cluster for the Main Master (MM) port accesses. It contains buffers that can handle direct cache-to-cache transfers between cores without having to read or write data to the L2 cache. Cache-line migration enables dirty cache lines to be moved between cores. There is no requirement to write back transferred cache-line data to the L2 cache.

CPU bridges

The CPU bridges control buffering between the cores within the Cortex-R82 processor.

Clock and power management

The cluster supports a set of power-saving modes that are controlled by an external power controller. The modes are selected through power-mode requests on P-Channels, for each of the cores, and a separate P-Channel for the Cortex-R82 processor. Clock gating is supported through Q-Channel requests from an external clock controller to the Cortex-R82 processor. The Q-Channels allow individual control of the SCLK, PCLK, and ATCLK clock inputs.

Instruction Fetch Unit

The Instruction Fetch Unit (IFU) fetches instructions from the Instruction Tightly Coupled Memory (ITCM), from the Low Latency RAM (LLRAM) port, or from the Main Master (MM) port. The IFU predicts the outcome of branches in the instruction stream and passes the instructions to the Data Processing Unit (DPU) for processing.

Data Processing Unit

The DPU decodes and executes instructions. It executes instructions that require data transfer to or from the memory system by interfacing to the Load Store Unit (LSU). The DPU includes the Generic Interrupt Controller (GIC) CPU interface, the Performance Monitoring Unit (PMU) and the Advanced SIMD and floating-point support.

GIC CPU interface

The GIC CPU interface, when integrated with an external distributor component, is a resource for supporting and managing interrupts in a cluster system.

PMU

The PMU provides six event counters that can be configured to gather statistics on the operation of each core and the memory system. The information can be used for debug and code profiling.

Advanced SIMD and floating-point support

Advanced SIMD is a media and signal processing architecture that adds instructions primarily for audio, video, 3D graphics, image, speech processing, and machine learning. The floating-point architecture provides support for half-precision, single-precision, and double-precision floating-point operations. The Advanced SIMD architecture, its associated implementations, and supporting software, are also referred to as Arm Neon™ technology.

Memory System

The Cortex-R82 processor memory system provides various memories and interfaces each tailored to different requirements. The aim is to use some memories and interfaces for more critical real-time requirements and some for less critical real-time requirements. However, the more real-time critical context is also able to access the less real-time critical interfaces and memories although such an access might not be desirable depending on the system design.



The Cortex-R82 processor has:

- + A shared Main Master (MM) port implemented as AXI5 256-bit providing access for instructions, data, and peripherals. This interface can optionally be a 256-bit CHI-E interface.
- + An optional AXI5 256-bit shared Low-latency RAM (LLRAM) port providing low-latency access for instructions, data, and peripherals. (Optional here means that the logic is always present, but it can be disabled.)
- + An ACE5-Lite 128-bit shared slave main Accelerator Coherency Port (ACP) for external access to MM address ranges. ACP enables I/O coherency for external agents with the per-core L1 data cache and shared L2 cache.
- + An optional AXI5 64-bit Shared Peripheral Port (SPP) for providing access to peripherals. (Optional here means that the logic is always present, but it can be disabled.)
- + A 128-bit shared AXI-S port used for two purposes:
 - As an LLRAM Accelerator Coherency Port enabling I/O coherent external access to the LLRAM port.
 - As a TCM slave enabling external agents to access the TCMs within the cores.
- + An optional, shared, and unified 8-way L2 cache. The L2 cache can cache instructions and data only from the MM port but not the LLRAM port. The L2 memory supports cache maintenance operations according to the Arm architecture and memory testing using MBIST.
- + 64-byte cache lines for the L2 cache.
- + RAM testing using MBIST.

Each core within the Cortex-R82 processor has:

- + An optional AXI5 32-bit Low-latency Peripheral Port (LLPP) for providing access to peripherals. (Optional here means that the logic is always present, but it can be disabled.)
- + An optional Instruction Tightly Coupled Memory (ITCM) with configurable size 0 Or from 16KB to 1MB in powers of 2. ITCM provides lowest-latency access for instructions and data. (Optional here means that the logic is always present, but the size can be 0.) ITCM is unified, that is, although it is optimized for instruction use, it is also available for data. Optional wait-states are supported.
- + An optional Data Tightly Coupled Memory (DTCM) with configurable size 0 or from 16KB to 1MB in powers of 2. DTCM provides lowest-latency access for data only. (Optional here means that the logic is always present, but the size can be 0.)

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- + Direct Memory Access (DMA) to all the TCMs in all cores via a TCM Slave port implemented through AXI-S. Optional wait-states are supported.
 - + 4-way L1 instruction cache with configurable size from 16KB to 64KB in powers of two that can cache instructions from the MM port or the LLRAM port.
 - + 4-way L1 data cache with configurable size from 16KB to 64KB in powers of two that can cache data with Write-Through caching for LLRAM locations and Write-Back caching for MM locations.
 - + 64-byte cache lines for both L1 instruction and L1 data caches.
 - + A Store buffer Unit (STU) for merging and forwarding (as appropriate) stores to TCMs (ITCM and DTCM), L1 caches, LLPP, SPP, LLRAM, and MM.
 - + 128-bit data path for loads and stores to caches and TCMs (ITCM and DTCM).
 - + Cache maintenance operations according to Arm architecture.
 - + RAM testing using MBIST.
 - + Optional Error Correcting Code (ECC) protection for all functional RAMs providing Single Error Correct Double Error Detect (SECCDED) scheme if there is a need to produce corrected data from error data or Double Error Detect (DED) scheme otherwise.

Memory Management Unit

The Memory Management Unit (MMU) implements the Virtual Memory System Architecture (VMSA) and is responsible for:

- + Controlling the translation table walk hardware that accesses translation tables in main memory.
- + Translating Virtual Addresses (VAs) to Physical Addresses (PAs).
- + Providing fine-grained memory system control through a set of virtual-to-physical address mappings and memory attributes that are held in translation tables.

Each stage of address translation uses a set of address translations and associated memory properties that are held in translation tables. Translation table entries can be cached into a Translation Lookaside Buffer (TLB).

The MMU includes the following components:

- + 15-entry, fully associative L1 instruction TLB.
- + 16-entry, fully associative L1 data TLB.
- + 1024-entry L2 TLB (256 sets of 4 ways).
- + 32-entry walk cache (8 sets of 4 ways).

The Cortex-R82 processor implements an EL1-MMU for EL0 and EL1 memory accesses. This MMU is optional and configurable on a per-core basis. Each Cortex-R82 core supports having both an EL1-MPU and EL1-MMU and software can choose which one to use. However, if no EL1-MPU is present, then an EL1-MMU must be present.

Memory Protection Unit

The Memory Protection Unit (MPU) implements the Protected Memory System Architecture (PMSA) and determines the attributes for each memory location including permissions, type, and cacheability.

Access permissions determine which levels of privilege are permitted to access a location and whether write access or instruction execution are permitted. Memory type and cacheability affect how the Cortex-R82 processor handles particular accesses, for example, if the processor permits two stores to be merged into a single write access.

The Cortex-R82 processor implements two programmable MPUs, EL1-MPU and EL2-MPU, controlled from EL1 and EL2 respectively. These MPUs are optional and configurable on a per-core basis. Each Cortex-R82 core supports having both an EL1-MPU and EL1-MMU and software can choose which one to use. However, if no EL1-MMU is present, then an EL1-MPU must be present. The EL2-MPU is optional but is required if virtualization at EL2 is to be used.

Debug and trace components

The Cortex-R82 processor supports a range of debug, test, and trace options including:

- + Per-core PMU to monitor events that happen within the core. Provides six performance event counters and one cycle counter.
- + Per-core debug logic providing six hardware breakpoints and four watchpoints.
- + Per-core ETM instruction and data trace on separate ATB buses:
 - An ATB4 32-bit bus for instruction.
 - An ATB4 128-bit bus for data and ELA.
- + The trace is generated per core, but the ATB buses are shared between the cores.
- + Support for a cluster level CoreSight ELA-600 Embedded Logic Analyzer to monitor the hardware signals related to the shared logic.

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- + Support for per-core CoreSight ELA-600 to monitor the hardware signals within the core. The configuration option to pre-integrate ELAs is global. (Note the CoreSight ELA-600 is a separately licensable product.)
 - + A cluster level PMU to monitor events that happen at the shared logic. Provides six performance event counters and one cycle counter.
 - + AMBA 4 APB interfaces between the cluster and the DebugBlock.

DebugBlock

The DebugBlock transfers trigger events to/from the Cortex-R82 processor.

The DebugBlock is separated from the Cortex-R82 processor to facilitate the following system design options:

- + The DebugBlock is placed in a separate power domain, to ensure that it is possible to maintain the connection to a debugger while the cores and cluster are powered down.
- + The DebugBlock is physically placed with the other CoreSight logic in the SoC, rather than close to the cluster.

The separate power domains allow the cores and the cluster to be powered down while maintaining essential state that is required to continue debugging. Separating the logical power domains into physical domains is optional and might not be available in individual systems.

System debug APB

The system debug APB slave interface connects to external CoreSight components, such as the Debug Access Port (DAP) to provide access to the Debug registers, ETM, and ELA in each core within the Cortex-R82 processor.

CTI and CTM

The DebugBlock implements Embedded Cross Trigger (ECT). A Cross Trigger Interface (CTI) is allocated to each core in the cluster. An additional CTI is allocated to the cluster PMU and, if present, to the cluster ELA. The CTIs are interconnected through the Cross Trigger Matrix (CTM). A single external channel interface is implemented to allow cross-triggering to be extended to the SoC.

Debug ROM Table

The Debug ROM table contains a list of components in the system. Debuggers can use the Debug ROM table to determine which CoreSight components are implemented.

Power management and clock gating

The DebugBlock implements two Q-Channel interfaces, one for requests to gate the PCLK clock and a second for requests to control the debug power domain.

Processor Interfaces

Name	Protocol	Width	Details
Low-latency Peripheral Port (LLPP)	AMBA 5 AXI	32-bit	Optional private LLPP per core for minimum latency access to memory and devices outside the cluster.
Generic Interrupt Controller (GIC) Stream interface	AMBA 4 AXI4-Stream	32-bit	AXI-4 Stream interface for interrupts between the Cortex-R82 processor and the system components.
DebugBlock	AMBA 4 APB	32-bit	APB interface between the Cortex-R82 processor and the DebugBlock.
Low-latency RAM (LLRAM)	AMBA 5 AXI	256-bit	Optional LLRAM for low latency access to memory shared between cores within the cluster.
Trace	AMBA 4 ATB	32-bit instruction ATB trace 128-bit data ATB trace	Two master ATB interfaces for instructions and data. An instruction trace funnel funnels all the processor ETM instruction trace streams into a single ATB trace bus. A data trace funnel funnels all the processor ETM data trace streams and all the ELA trace streams into a single ATB trace bus.
Utility bus	AMBA 5 AXI	64-bit	Manages power states and provides access to Power Policy Units (PPUs) registers and Reliability, Availability, and Serviceability (RAS) registers in each core and the cluster.

AXI-S	AMBA ACE5-Lite	128-bit	Enables external agents to access to the TCMs and LLRAM port.
WFE event signaling	-	-	Signals for Wait-For-Event (WFE) wake-up events.
Clock state control	Q-Channel	-	Q-Channels for clock gating control.
Power state control	P-Channel	-	P-Channels for Cortex-R82 processor power management.
Main Accelerator Coherency Port (ACP)	AMBA 5 ACE-Lite	128-bit	Provide access to the MM port to external masters.
Shared Peripheral Port (SPP)	AMBA 5 AXI	64-bit	Optional shared SPP for minimum latency access to memory and devices.
Main Master (MM)	AMBA 5 AXI or CHI	256-bit	Shared MM port for accesses to high-latency memory and non-critical peripherals.
Generic Timer	-	-	Input for the Generic Timer counter value. The counter value is distributed to all cores. Each core outputs timer events.
Design for Test (DFT)	-	-	Interface to support access for Automatic Test Pattern Generation (ATPG) scan-path testing.

DebugBlock Interfaces

Name	Protocol	Details
External debug	AMBA 4 APB	Slave interface to external debug component, for example a Debug Access Port (DAP). Allows access to Debug registers and resources.
DebugBlock	AMBA 4 APB	APB interface between the Cortex-R82 processor and the DebugBlock.
Cross-trigger channel interface	CTI	Allows cross-triggering to be extended to external SoC components.
Power management	Q-Channel	Enables communication to an external power controller to control clock gating and power-down.

Cortex-R82 Configuration Options

Feature	Options
Cache protection	No RAM protection included. RAM protection included.
ELA	No ELA included. ELA included.
L2 cache size	No L2 cache. L2 cache present with size of 128KB, 192KB, 256KB, 384KB, 512KB, 768KB, 1024KB, 1536KB, 2048KB, 3072KB, or 4096KB.
L2 cache data RAM input latency	1-cycle latency. 2-cycle latency. 2-cycle latency with an extra hold cycle.
L2 cache data RAM output latency	2-cycle latency. 3-cycle latency.
L2 cache data RAM output register slice	No register slice. Register slice included.
L2 cache data RAMs clock pulse stretch	Stretched. Not stretched.
Power on reset state for the Power Policy Units (PPUs)	Cluster and all core PPU's reset to off. Cluster and core 0 PPU's reset to on. Any other core PPU's reset to off. Cluster and all core PPU's reset to on.
Number of EL2 Memory Protection Unit (MPU) regions	0, 16, or 32
Number of EL1 MPU regions	0, 16, or 32
Main master bus type	Main master is AXI-5. Main master is CHI.
VMSA support	EL1-MMU included. EL1-MMU not included.
Advanced SIMD and floating-point support	No Advanced SIMD and no floating-point support included. Advanced SIMD and half precision, single precision, and double precision floating-point functionality included.
Number of wait states incurred by accesses to the ITCM	0, 1, 2, 3
ITCM clock pulse stretch	Stretched. Not stretched.
Data Tightly Coupled Memory (DTCM) size	0 (DTCM logic is always present but the size can be 0), 16KB, 32KB, 64KB, 128KB, 256KB, 512KB, 1024KB.
Instruction Tightly Coupled Memory (ITCM) size	0 (ITCM logic is always present but the size can be 0), 16KB, 32KB, 64KB, 128KB, 256KB, 512KB, 1024KB.
Number of wait states that are incurred by accesses to the DTCM	0, 1, 2, 3
DTCM clock pulse stretch	Stretched. Not stretched.

Supporting technical documents coming soon.

Learn more about the processor [here](#).

Glossary of Terms

CTI	Cross Trigger Interface
CTM	Cross Trigger Matrix
DAP	Debug Access Port
DED	Double Error Detect
DFT	Design for Test
DMA	Direct Memory Access
DPU	Data Processing Unit
DTCM	Data Tightly Coupled Memory
ECC	Error Correcting Code
ECT	Embedded Cross Trigger
ELA	Embedded Logic Analyzer
ETM	Embedded Trace Macrocell
GIC	Generic Interrupt Controller
IFU	Instruction Fetch Unit
ITCM	Instruction Tightly Coupled Memory
LLRAM	Low-latency RAM
LLPP	Low-latency Peripheral Port
LSU	Load Store Unit
MACP	Main Accelerator Coherency Port
MBIST	Memory Built-In Self-Test
ML	machine learning
MM	Main Master
MMU	Memory Management Unit
MPU	Memory Protection Unit
PMU	Performance Monitoring Unit
PMSA	Protected Memory System Architecture
PPUs	Power Policy Units
RAS	Reliability, Availability, and Serviceability
SB	Snoop Control Unit Bridge
SCP	System Control Processor
SECEDED	Optional Single Error Correct Double Error Detect
SIMD	Single Instruction Multiple Data
SPP	Shared Peripheral Port
STU	STore buffer Unit
TCMs	Tightly Coupled Memories

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