HPCG Preliminary Evaluation on A64FX

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Disclaimer

- The software used for the evaluation, such as the compiler, is still under development and its performance may be different when the supercomputer Fugaku starts its operation.

- The result of the RIKEN post-K processor simulator is just an estimated value, and it does not guarantee the performance of the supercomputer Fugaku at the start of its operation.
- Kodama etc., “Evaluation of the RIKEN Post-K Processor Simulator,”
Background of Our Research

- We have been developing CPU simulator for “A64FX”
  - “RIKEN Fugaku Processor Simulator and its Accuracy for Cache and Memory Throughput”, Yuetsu Kodama (RIKEN R-CCS), Arm Research summit 2019
- The result of Stream Triad demonstrate the accuracy of the simulator by showing that the difference between our simulator and A64FX test chips is approximately 10%
  - Caches and memory bandwidth
- In this research, we show the results on the performance evaluation of HPCG benchmark
HPCG Benchmark

- HPCG is intended to model the data access patterns of real-world applications
  - Solving symmetric sparse linear system equations by using the CG (conjugate gradient) method preconditioned with multi-grid symmetric Gauss-Seidel smoother

- Official runs of HPCG must be at least 1800 seconds and need much memory usage

- Since the execution by simulator is very slow, the problem size must be minimized as to finish the execution within a few hours
Evaluation Environment; RIKEN Simulator

- **HPCG by Arm**
  - NEON; Tuning for NEON
  - SVE_INTRINSICS; Tuning for SVE with ACLE (Intrinsic)
  - SVE_WO_INTRINSICS; Tuning for SVE

- **Problem size**
  - nx = ny = nz = 32 (too small !!!)
  - QuickPath enabled

- **Compiler**
  - Fujitsu compiler (FCCpx); prototype compiler for the "Fugaku"
    - Options: -Kfast,openmp
  - Arm compiler 19.1 (armclang++)
    - Options: -O3 -fopenmp -std=c++11 -march=armv8.1-a+sve -ffast-math
Result of HPCG by RIKEN Simulator

- SVE performances are higher than that of NEON
- There is no significant difference in performance because the problem size is small
Evaluation on A64FX Test Chip

- Recently, we can access A64FX test chips (real hardware!) to evaluate its performance
- Evaluating the performance of HPCG and the difference between our simulator and test chip

Spec of A64FX
- Armv8.2-A+SVE and Fujitsu extensions
- SVE 512-bit, also NEON 128-bit
- 12-cores x 4-CMGs (= 48-cores)
- HBM2; 256GB/s/CMG (Total 1,024GB/s)
Evaluation Environment on A64FX

- **HPCG by Arm**
  - NEON; Tuning for NEON
  - SVE_WO_INTRINSICS; Tuning for SVE
  - SVE_INTRINSICS; Tuning for SVE with ACLE (Intrinsic)

- **Problem size**
  - \( nx = ny = nz = 64 \)
  - QuickPath enabled

- Note that cache hit-rate may be high due to small problem size
- Note that compilers are still under development and may not perform as expected
Evaluation on A64FX

- SVE dose not affect this evaluation
- Storage format?, Small problem size?
- Using compiler optimization allows better performance than using user’s ACLE
Compiler Optimization for A64FX

- **Software pipelining (SWP)**
  - Optimization method that Fujitsu has been good at since K computer
  - The live range (time) of values in hardware registers may became short, resulting in better IPC (Instructions per cycle) can be increased by rearranging instructions
    - $\rightarrow$ FPU usage is increasing

- **Loop unrolling (Unroll)**
  - Traditional optimization method
  - Combined with SWP, IPC can be more increased
Effects of Compile Optimization

- **X1.8~2.0 enhanced!**
- **Unroll and SWP improve the performance from 1.8 to 2 times perf in NEON**
- **In this case, loop unrolling is particularly effective**

There is no difference in SVE code
Accurate of RIKEN Simulator

- Differences of NEON are larger than SVE
- SVE of Fujitsu compiler are almost the same
Conclusion and Future Work

- We have evaluated the performance of HPCG by RIKEN simulator and A64FX test chip
  - In the benchmark closed to real applications, there was still difference between our simulator and the test chip, especially in NEON
  - Fujitsu compiler’s optimizations achieve high performance

- We will evaluate larger problem size
- Investigate why SVE does not improve the performance, and how to use ACLE