



EPI Processor

20190915 - Arm Research Summit 2019

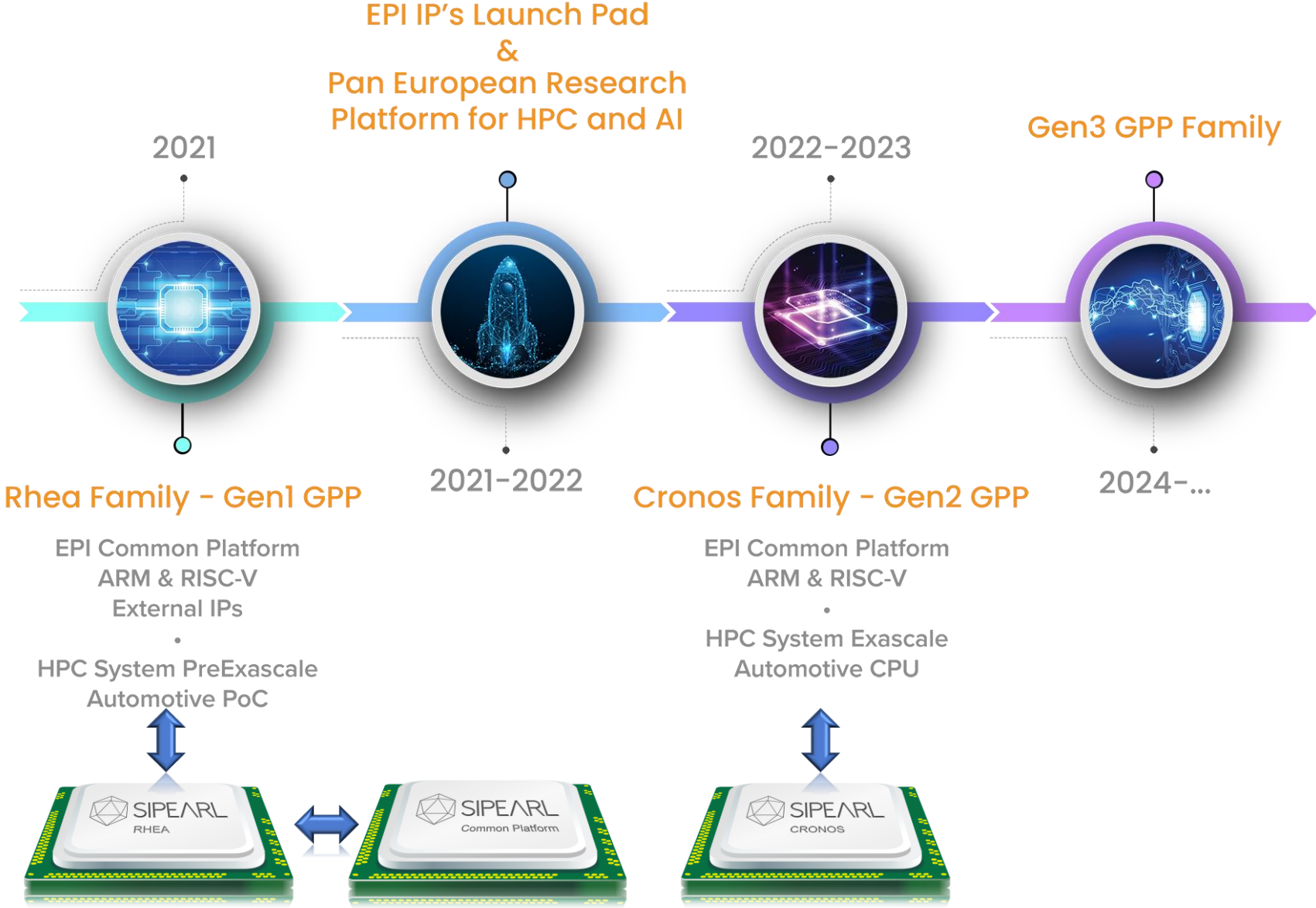
Yingchih YANG, EPI Lead Architect

EPI Project and EPI processor

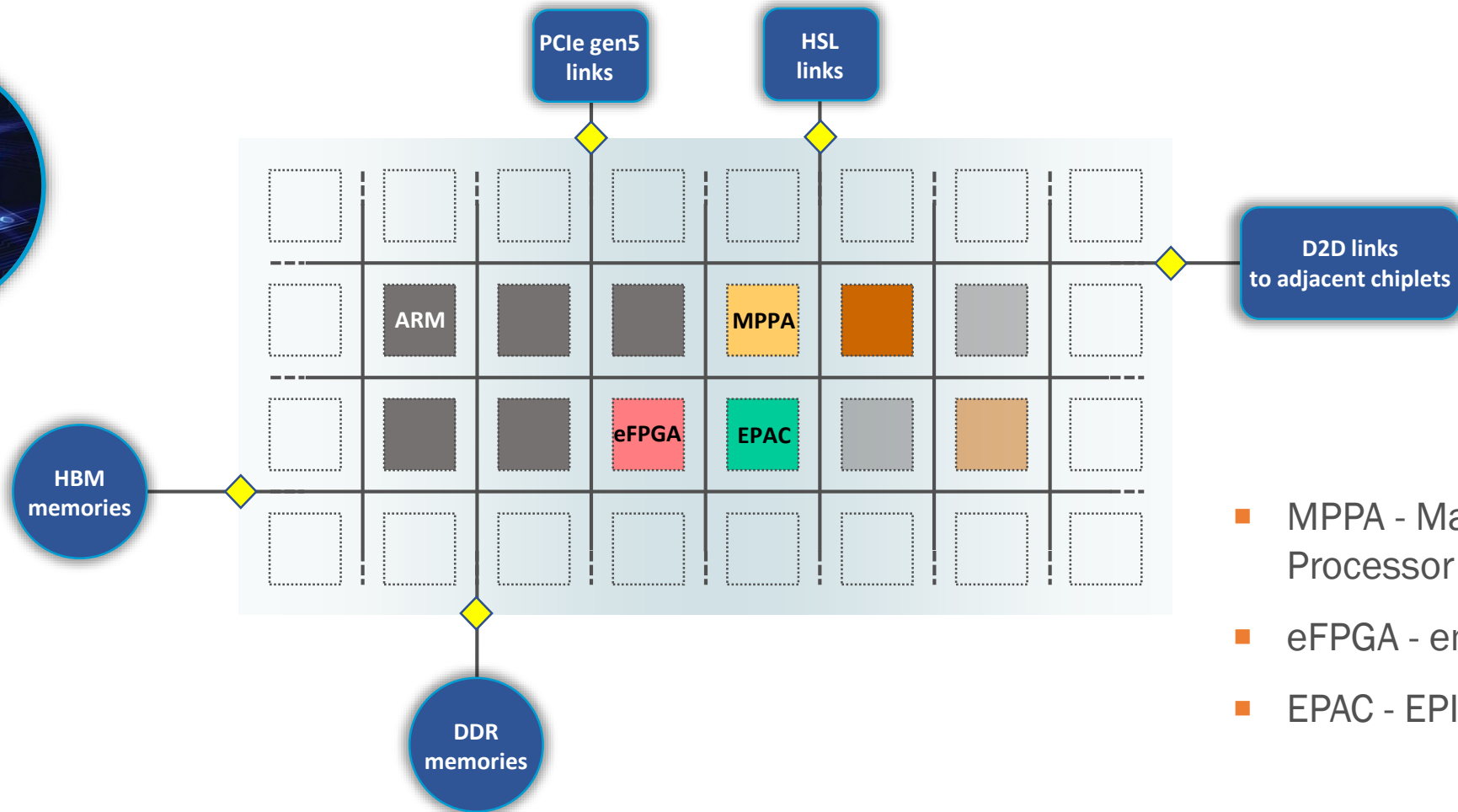
- European Processor Initiative (EPI) is an EU H2020 Project
 - To design a roadmap to foster low-power high-performance processor technologies
 - 26 EPI partners in 3 streams : GPP chip for HPC application, acceleration technologies and automotive application
 - EPI carries on the activities in previous Mont Blanc projects
- SiPEARL is the entity that
 - Developing the first EPI GPP processor implementation
 - Aligning its schedule with EuroHPC timeline
 - Promoting its eHPC use in automotive applications

GPP : General-Purpose Processor

SiPEARL – Roadmap



GPP and Common Platform



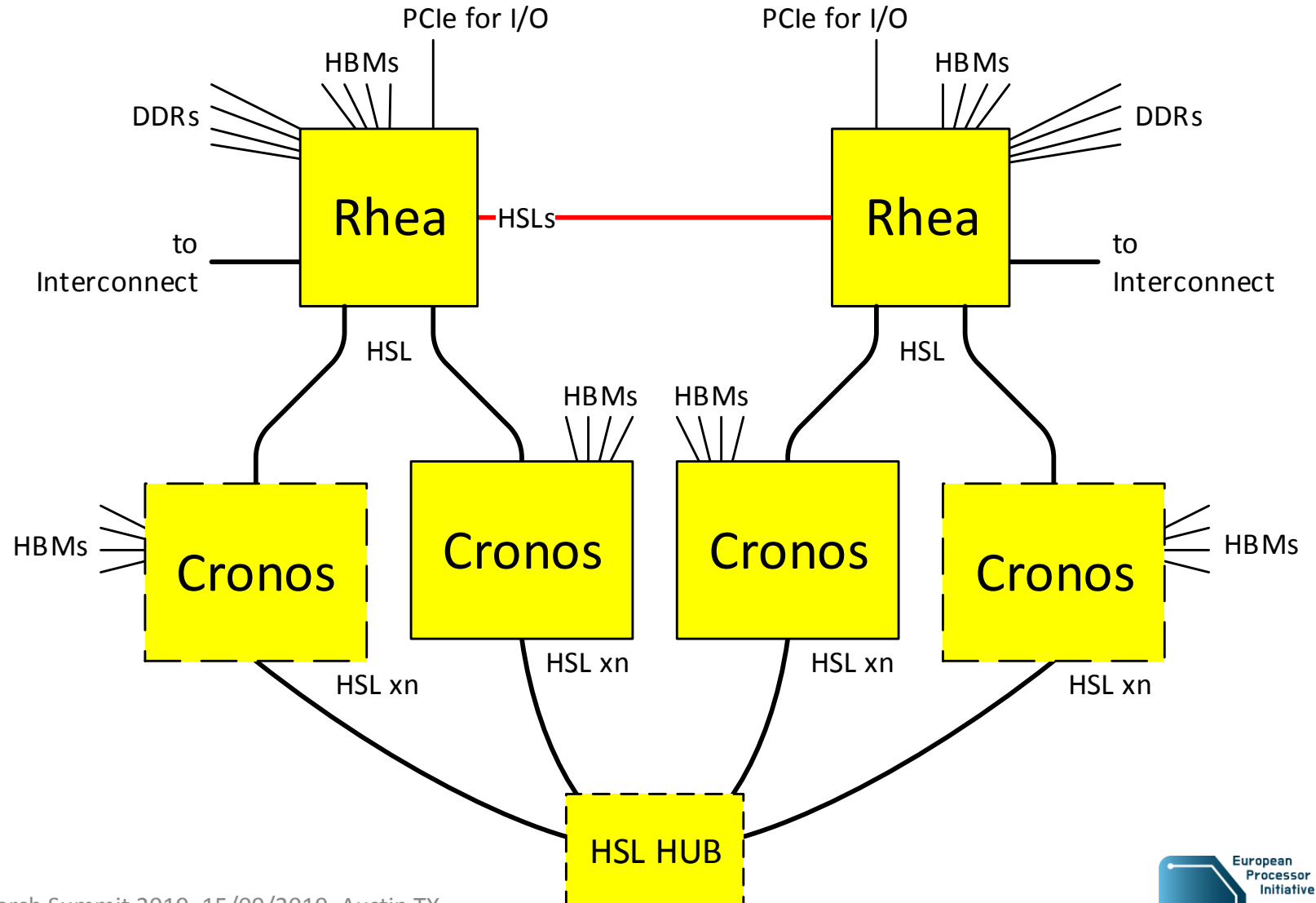
- MPPA - Massively Parallel Processor Array
- eFPGA - embedded FPGA
- EPAC - EPI Accelerator

Rhea designs

- Multi-core Armv8 processor with SVE engines for both control flow and computing
- EPI Accelerators work in I/O coherent mode and share the same memory view
- Coherent NoC with system level cache to keep the data local
- HBM2E, DDR5 and PCIe gen5
- CCIX for SMP and for functional extensions
- Low voltage to improve the energy efficiency

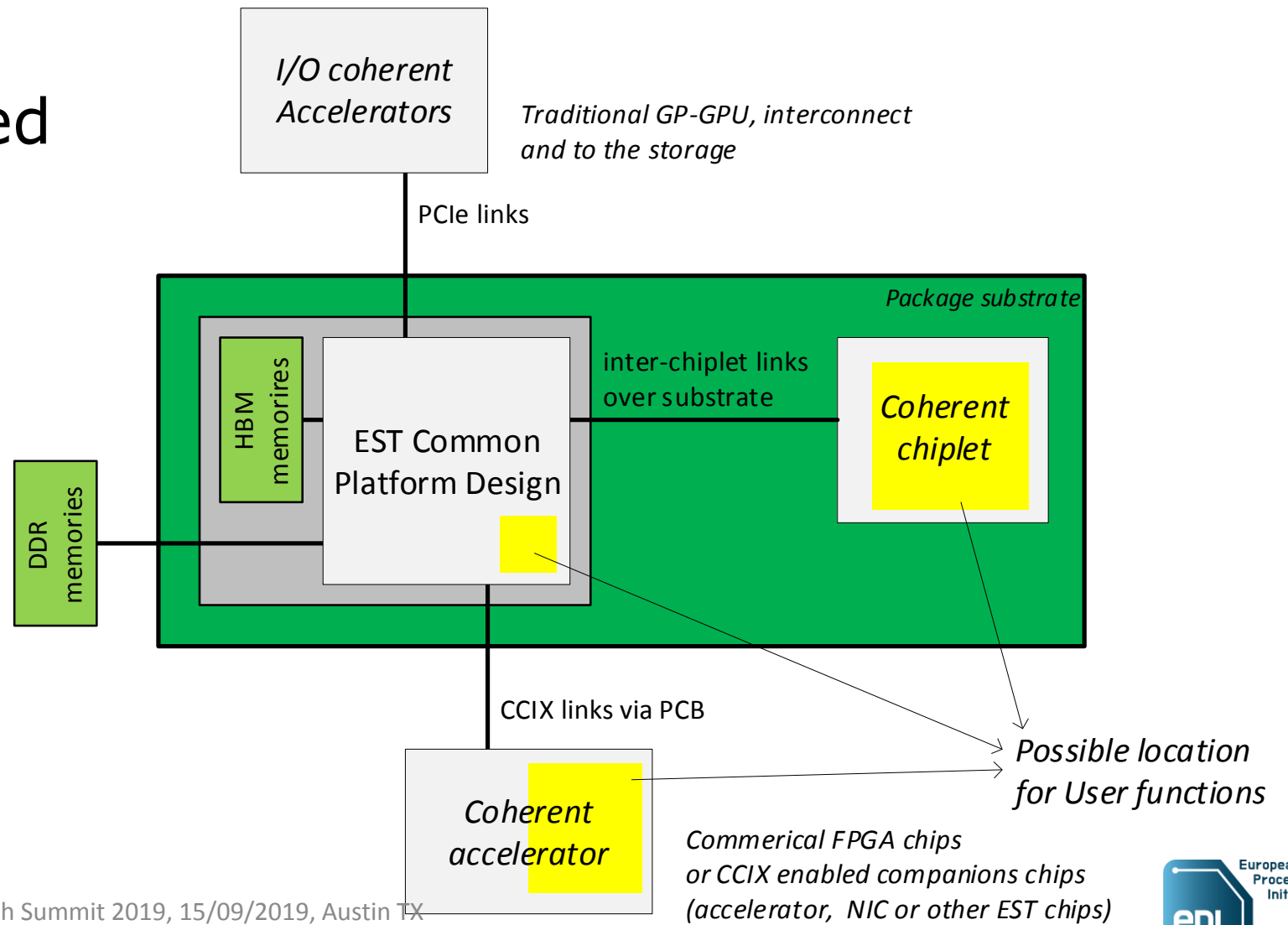
EPI roadmap for HPC

- gen1 / Rhea
 - General purpose
 - Homogeneous
 - Interconnect
 - Memory and storage
- gen2 / Cronos
 - Accelerated
 - Heterogeneous



Heterogeneous Integration

- Integrating customized functions at different levels
 - EPI accelerator IPs today is integrated in RheaR1 design



Challenges

- Programming model for Data-centric processing
(or 'off-loading' from GPP point of view)
- GFLOPS/\$ vs. GFLOPS/Watt vs. single-thread performance

GFLOPS/\$

= Gigahertz frequency

* FLOPs/cycle

/ # of transistors (Mgate)

/ unit transistor cost (\$/Mgate)

GFLOPS/Watt

= Gigahertz frequency

* FLOPs/cycle

/ Power (Watt)