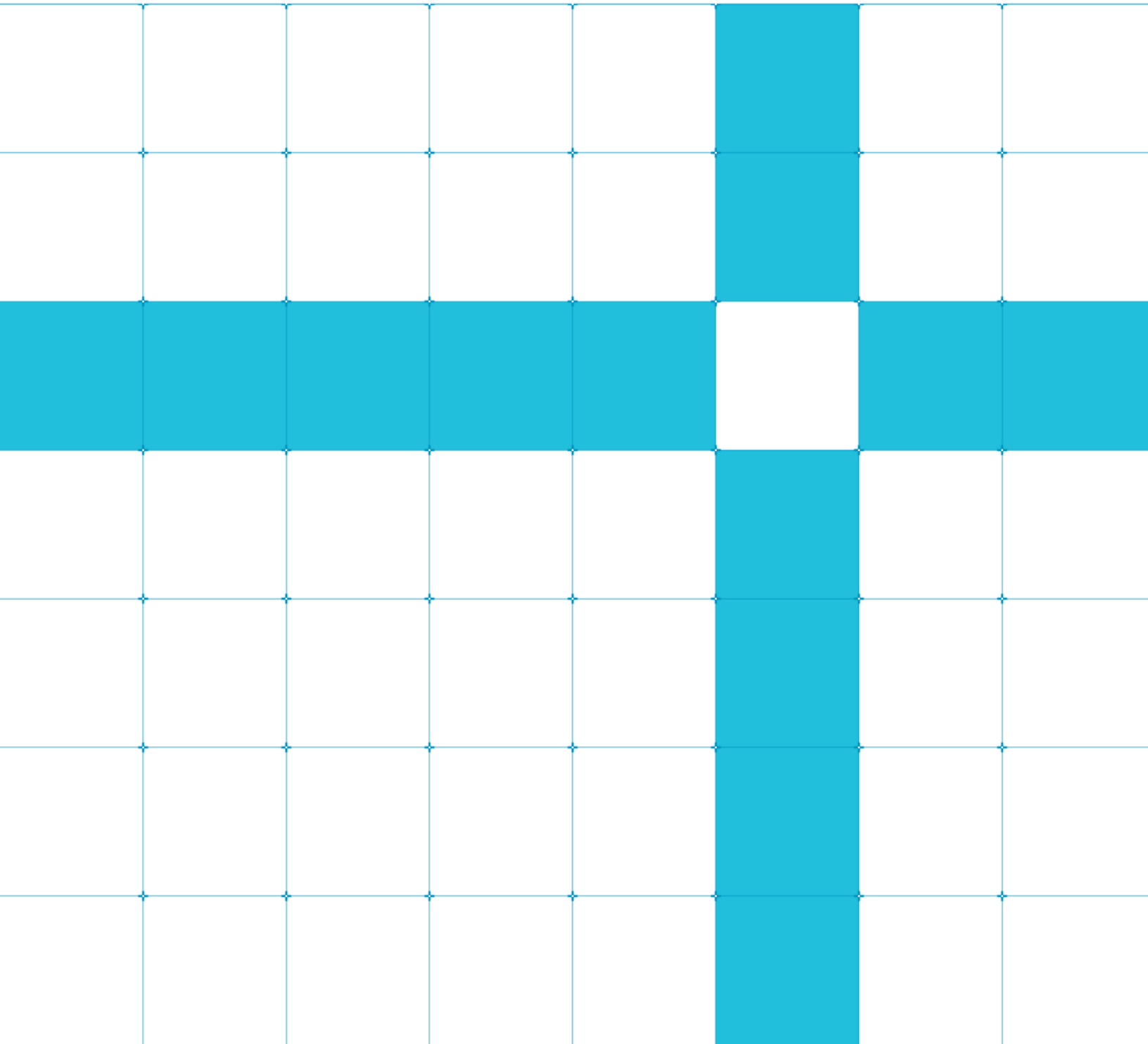# arm

Understanding the Armv8.x extensions

Version 1.0

Understanding the Armv8.x extensions

Learn the architecture guide

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Release Information

Document History

Version	Date	Confidentiality	Change
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The information in this document is Final, that is for a developed product.

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Contents

1 Overview

Additions to the Arm architecture are provided as version increments known as extensions. Extensions allow us to release new features regularly in response to the needs of our partners without making major changes to the main architecture.

We release a new extension every year. In line with this, our Cortex CPUs, which are our implementations of the architecture, utilize the latest extension depending on when they are released.

This guide explains extensions to the Arm architecture and provides guidance on how to read and use them.

At the end of this guide, you can check your knowledge. You will have learned how the extensions are expressed, which features are available in which extensions, and how to determine which features of extension an Arm Cortex CPU implementation supports.

2 What does Armv8.x-A mean?

There are different versions of the Arm architecture. These different versions are usually shown as ArmvX, in which X is the version number. For example, Armv8-A means version 8 of the Arm A-profile architecture. A version such as Armv8-A is a major release of the architecture.

However, there are also minor versions that are added to a major release. These minor version are called .x extensions. For example, Armv8.1-A means version 8 of the A-profile architecture, extended by the .1 extension.

3 Why do we need the .x extensions?

Development of major versions of the Arm architecture can take many years. For example, Armv7-A was released in 2007 and Armv8-A followed six years later, in 2013. Because architecture needs to evolve between major versions to add new features, minor versions, the *.x extensions*, are added.

Since the release of Armv8-A, the process of adding to the architecture between major versions has been formalized. There is now an annual release of a .x extension. Beginning with Armv8.0-A, the base specification, the Armv8.1-A extension was added in 2015, the Armv8.2-A extension was added in 2016, and so on. Each .x extension builds on the last, so that Armv8.2-A includes all the features of Armv8.1-A, and adds new features.

Each .x extension is relatively minor. The *Arm Architecture Reference Manual* (Arm ARM) for the base specification, and original release, is approximately 6,000 pages long. By comparison, the Armv8.3-A specification is only 48 pages long.

4 Processor implementation of Armv8.x-A

Each .x extension includes a set of features, some mandatory and some optional. A processor implements a .x extension if it implements all the mandatory features of that extension number, and those from all previous extensions.

For example, to be described as implementing Armv8.2-A, a processor must implement all the mandatory features from:

- Armv8.0-A - the base specification and original release.
- Armv8.1-A - the previous extension.
- Armv8.2-A - the new extension.

Note: A feature might originally be optional, but later become mandatory. For example, the Dot Product instructions were optional in all extensions from Armv8.0-A to Armv8.3-A, but became mandatory in Armv8.4-A.

5 Feature implementation between Armv8.x versions

An Armv8.x-A processor can implement any features from the next .x extension. However, it cannot implement features from any .x extension after that.

For example, a processor described as implementing Armv8.1-A:

- Must implement all the mandatory features of Armv8.0-A and Armv8.1-A.
- Is permitted to implement some features from Armv8.2-A.
- Is not permitted to implement features from Armv8.3-A, Armv8.4-A, and so on.

6 Armv8.x extensions and features

Here we summarize the new features that were added in each of the Armv8.x-A extensions. We do not provide a complete list, but we include the most important features. Notice that some features are limited to the AArch64 state, and others are available in both the AArch32 and AArch64 states.

Note: AArch32 is a 32-bit Execution state that is supported in all versions of Arm architecture before Armv8-A. AArch64 is a 64-bit Execution state and is supported only in the Armv8-A architecture.

Armv8.1-A

- Atomic memory access instructions (AArch64)
- Limited Order regions (AArch64)
- Increased Virtual Machine Identifier (VMID) size, and Virtualization Host Extensions (AArch64)
- Privileged Access Never (PAN) (AArch32 and AArch64)

Armv8.2-A

- Support for 52-bit addresses (AArch64)
- The ability for PEs to share Translation Lookaside Buffer (TLB) entries (AArch32 and AArch64)
- FP16 data processing instructions (AArch32 and AArch64)
- Statistical profiling (AArch64)
- Reliability Availability Serviceabilty (RAS) support becomes mandatory (AArch32 and AArch64)

Armv8.3-A

- Pointer authentication (AArch64)
- Nested virtualization (AArch64)
- Advanced Single Instruction Multiple Data (SIMD) complex number support (AArch32 and AArch64)
- Improved JavaScript data type conversion support (AArch32 and AArch64)
- A change to the memory consistency model (AArch64)
- ID mechanism support for larger system-visible caches (AArch32 and AArch64)

Armv8.4-A

- Secure virtualization (AArch64)
- Nested virtualization enhancements (AArch64)
- Small translation table support (AArch64)
- Relaxed alignment restrictions (AArch32 and AArch64)
- Memory Partitioning and Monitoring (MPAM) (AArch32 and AArch64)
- Additional crypto support (AArch32 and AArch64)
- Generic counter scaling (AArch32 and AArch64)
- Instructions to accelerate SHA512 and SHA3 (AArch64 only)

7 Which .x extension does my processor implement?

The Arm architecture includes a set of feature registers that report the features supported by the processor. For each new feature added by a .x extension, even the optional features, a field in these feature registers reports whether it is supported or not.

For example, `ID_AA64MMFR2_EL1.AT` tells you whether there is support for the relaxed alignment requirements in Armv8.4-A. What you will not find is a field that reports that this processor is Armv8.1-A. Software reads the feature fields for the mandatory 8.1-A features, and if they all present, the processor is compliant with Armv8.1-A.

Arm Cortex-A processors

For the Cortex-A processors released at the time of writing, this table summarizes which .x extensions are supported by which processor.

Architecture	Processors
Armv8.0-A	Cortex-A32
	Cortex-A35
	Cortex-A53
	Cortex-A57
	Cortex-A72
	Cortex-A73
Armv8.2-A	Cortex-A55
	Cortex-A75
	Cortex-A76

Note: At the time of writing, no Armv8.3-A, or Armv8.4-A Cortex processors are available.

8 Armv8.x-A and the SBSA

The *Server Base System Architecture* (SBSA), provides hardware requirements for servers. The SBSA ensures that operating systems, hypervisors and firmware operate correctly. For servers, where a degree of standardization is important, the SBSA includes rules on which extensions to the architecture must be implemented.

The following table summarizes the SBSA requirements that relate to the Armv8.x-A extensions:

Version	Feature	SBSA		
		Level 3	Level 4	Level 5
Armv8.0-A	Advanced SIMD	Mandatory		
	Crypto instructions	Mandatory (subject to export restrictions)		
	CRC	Mandatory		
	4KB and 64KB granule	Mandatory		
	16 bit ASID	Mandatory		
	EL2 and EL3	Mandatory		
	AArch64 at all Exception Levels	Mandatory		
	At least 6 PMUY counters	Mandatory		
	At least 6 breakpoints and four synchronous watchpoints	Mandatory		
Armv8.1-A	16-bit VMIDs	-	Mandatory	
	Virtualization Host Extension	-	Mandatory	
Armv8.2-A	RAS	-	Mandatory (at least minimal implementation)	
	Persistent memory	-	Optional (with restrictions)	
Armv8.3-A	Nested virtualization	-	-	Optional (with restrictions)
	Pointer authentication	Optional (with restrictions)	Mandatory	
Armv8.4-A	Stage 2 type overrides	-	-	Mandatory
	Enhanced nested virtualization	-	-	Mandatory
	Activity monitors	-	-	Mandatory
	MPAM	-	-	Optional (with restrictions)
	SHA3 and SHA512	-	-	Mandatory (subject to export restrictions)
	Generic counter scaling	-	-	Mandatory

9 Check your knowledge

Q. What are the major version and .x extension in Armv8.3?

A. 8 is the version, and 3 is the .x extension.

Q. Secure virtualization was added in Armv8.4-A. Would an Armv8.1-A processor be allowed to implement it?

No. An Armv8.1 processor must implement the mandatory features of Armv8.1 and may implement features from Armv8.2-A. But it is not allowed to implement features from Armv8.3, Armv8.4, or later versions, unless a special concession has been made.

Q. Is this sentence true or false? Only optional features have fields to report their presence.

A. False. Mandatory and optional features have fields to report their presence.

Q. Which major version and extension of the Arm architecture does the Cortex-A55 implement?

A. Armv8.2-A.

Q. Which level or levels of the SBSA require support for 16-bit VMIDs?

A. Level 3 and above.

10 Related information

To learn more about the following features referenced in this guide, refer to:

- *Synchronization guide* (coming soon).
- *Pointer signing and landing pads guide* (coming soon).
- *Security guides* (coming soon).
- *Armv8-A Virtualization* (coming soon).

Here are some resources related to material in this guide:

- Arm architecture and reference manuals (for information on Armv8.1-A, Armv8.2-A, Armv8.3-A, Armv8.4-A)
- Arm community (ask development questions, and find articles and blogs on specific topics from Arm experts)

Here are some resources related to topics in this guide:

Armv8-x.A and the SBSA

- Server Base System Architecture (SBSA)

11 Next steps

Every year, Arm releases extensions to its main architecture, in order to regularly release new features in support of partner needs. In this guide, we explained the extensions to the Armv8.x architecture, described how to read and use the extensions, and outlined some of the features that the extensions support.

After reviewing this guide, you should understand how the extensions are expressed, which features are available in which extensions, and how to determine which features an Arm Cortex CPU implementation supports.

To keep learning about the Armv8-A architecture, see more in our series of guides.