Arm Cortex-A Physical Implementation

Summary
This course is designed to help implementation engineers with the physical layout and implementation flow specific to their individual piece of Arm Cortex-A Processor IP, such as the Arm Cortex-A76 or Cortex-A65AE. Please note this course will need repeating for each separate processor when working on a multiple processor implementation.

At the end of the course, attendees will be able to

- **Describe** the design structure and configurable options
- **Analyse** clock and reset scheme
- **Use** the implementation methodology
- **Apply** timing constraints and data flow
- **Integrate** Power Grid and Low Power implementation
- **Learn** floorplan and placement guides from Arm experience
- **Analyse** critical timing and power consumption.
- **Integrate** DFT and MBIST

Prerequisites:
- A working knowledge of implementation flows.
- Experience of EDA tool operation.

Audience:
Engineers who work on a SoC project looking to carry out the physical implementation of Cortex-A processors

Length:
Two 3-hour Virtual Live Classroom sessions (WebEx) or 1-day private face to face per Arm Processor

Agenda

- Introduction
- RTL and Library Preparation
- Physical Implementation Flow
- Clocks and Resets
- Asynchronous Bridge and Timing Constraints
- Floorplan
- RAM requirement
- Timing Closure
- Major Function Units
- Power Grid Structure and Analysis
- DFT and MBIST