arm Training

Arm Neoverse – DynamIQ (CHI) System Design

Summary:
This training course covers system-wide configuration and integration topics for DynamIQ-based infrastructure systems. By the end of the course delegates will be able to:

- **Describe** the DynamIQ (DSU), Neoverse Processor main functions.
- **Integrate** the DSU in their SoC and configure to match their system requirements, including integrating GIC-600.
- **Explain** the DynamIQ (DSU) transaction flows and clocking schemes.
- **Describe** the DSU memory system configuration and behavior with different memory types.
- **Understand** the DSU and Neoverse processor power and reset modes and power transition flows.
- **Explain** DSU Debug and Trace integration.
- **Run** the supplied test cases when they get the release package testbenches.

Prerequisites:

- A working knowledge of SOC and RTL design.
- Intro to Arm online training (included)
- Armv8-A Overview (included)
- Introduction to DynamIQ online training (included)
- CHI training

Audience:

Engineers who work in a SoC project using Neoverse-N1 and carry out System Design or IP / SoC verification.

Length:

3 days

Modules:

Pre-course Online Training

- Introduction to Arm, Introduction to DynamIQ and Arm Cortex Processor Behaviors

Day 1-3

- DSU Infrastructure (CHI) System Design
- DSU Overview (Infrastructure / CHI)
- CMN-600 Overview
- CMN-600 CML Overview (optional)
- DSU / CMN-600 Transaction Flows
- Memory system configuration for DSU Infrastructure (CHI) Systems
- CMN-600 System Address Map
- CMN-600 Integration for DSU Infrastructure (CHI) Systems
- Integrating System-wide ARMv8.2 Support in DSU Infrastructure (CHI) Systems
- Integrating GIC-600 into a DSU Infrastructure (CHI) System
- DSU Clock Domains and Clock Gating
- DSU Power Domains and Power Modes
- DSU Power Mode Transitions and Reset Scenarios
- DSU Debug and Trace Integration
- CMN-600 Debug, Trace, and PM