arm Training

System MMU

Summary

System Memory Management Units (SMMUs) allow initiators to operate in a virtual address space.

At the end of this course, delegates will be able to

- Understand the Armv8 principles for virtualization and address translation (VMSA)
- Understand the SMMU (v2 or v3) architecture and consult the SMMU specification document to find relevant detailed information
- Define basic programming sequences for an SMMU (v2 or v3) implementation
- Configure and integrate an Arm SMMU implementation (MMU-500, MMU-600, MMU-600AE or MMU-700) based on system/application requirements
- Interpret transactions being issued by the Arm SMMU of choice (MMU-500, MMU-600, MMU-600AE or MMU-700) in the system

Prerequisites:

- A basic knowledge of the AXI/ACE protocol. If necessary, the class can be extended to cover these protocols.
- System integration knowledge

Audience:
Engineers who work on a SOC project and take charge of an Arm SMMU configuration and integration. Also, engineers who oversee Arm SMMU bring-up or full-SOC verification.

Versions:
This class is available in the following alternative variations:

- SMMUv2 and MMU-500
- SMMUv3.1 and MMU-600
- SMMUv3.1 and MMU-600AE
- SMMUv3.2 and MMU-700

Length:
Depending on the selected version, duration is between 6 hours and 10 hours.

Modules:
Armv8 memory management principles and VMSA

- Memory management principles
- Address translation process in Arm VMSA
- Translations at EL1/0
- Translations at EL2
- TLB maintenance

SMMU SW Architecture

- Introduction to the SMMU
- SMMU architecture evolution
- Operation of an SMMU
- SW interaction with the SMMU

SMMU HW (MMU-500, MMU-600, MMU-600AE or MMU-700)

- Topology and building blocks
- Block interfaces
- Operation and caching
- Internal structures
- RAM integration

- Configuration options

MMU-600AE Safety Mechanisms (if choosing MMU-600AE)

- Overview of the different Safety Mechanisms
- Integration aspects

DTI (optional)

- The DTI protocol and its relevance
- DTI messages description
- DTI messages in relation to Arm SMMU operation