arm Training

Arm-Cortex-A-Hardware Design

Summary

Arm Cortex-A Hardware training courses are designed to help engineers working on new or existing Cortex-A system designs. Whether you're working on design integration or verification, for a Cortex-A system, the course can be **configured according to your team's experience and relevant Arm IP**.

Courses are built around processor cluster specific hardware integration topics focusing on the needs of the RTL integration and verification team. The rest of each course can then expand on this with the architectural fundamentals necessary for the RTL verification team. The courses can be tailored based on the intended audience. Some key topics are delivered via **pre course on-demand video**.

A **pre course call** with the engineer delivering the training will help you discuss your team's individual training requirements and to identify the material specific to your needs.

At the end of the course delegates will be able to:

- Describe different Cortex-A processors features and their use.
- Identify and solve key Cortex-A system design issues.
- Make appropriate system design choices.
- Decide on the best configuration options for their system.
- Debug simulation issues on Cortex-A processors.

Course Length	Delivery Method	Location
2 – 4 days	Classroom	Virtual or Onsite

Audience

- RTL integration team
- RTL verification team
- System designers

Prerequisites

- Basic understanding of Verilog
- Basic programming experience (but it does not have to be ARM programming)

Related Products

Arm DynamIQ, Cortex-X1, A78, A77, A76, A75 A65, A57, A55, A53, A35, A34, A32, A17, A15, A9, A7, A5, CHI, ACE

Topics

Agendas will be created from the following list of integration and verification topics

Processor Cluster Specific Topics

- The memory access behaviour considering both the innate behaviour and the hardware control and configuration available
- The interaction between the processor and the system, and the expected connectivity and controls for the system interaction
- The behaviour and connectivity of the interrupt controller for the processor
- The debug capability behaviour for the processor and how it interacts with the system debug infrastructure.
- The design and system control of the processor clock, reset and power management

Cortex-A Verification Specific Topics

- **Introduction to the basics of the Arm Architecture and Assembly programming**. A discussion of the programmer's model, register layout and architectural features and the basics of the instruction set
- **Interrupt** and **exception** architecture, including how to handle IRQs and internal faults and how to program the interrupt controller.
- **Cortex-A memory model,** covering Arm memory types, interactions with caches and how to program the Memory Management Unit (MMU)
- How the Arm architecture requirements translate into the design of a Cortex-A processor and therefore the typical **Cortex-A processor behaviours** will cause interaction with a system.
- The implication of shared memory and devices in the system and its requirements for memory access **Coordination** and **cache coherency** for the Cortex-A processor
- Basic requirements of the protocol used for the main Cortex-A processor interfaces (As appropriate)
    - ACE
    - AXI
    - CHI

Related face-to-face and on-demand courses

- CoreSight Training
- Physical Implementation