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EXCELENCIA SEVERO OCHOA

Student Cluster Competition 2016

Universitat Politècnica de Catalunya (Spain) team

Filippo Mantovani

Senior researcher

14 Nov 2016

ARM HPC User Group

SC16 Salt Lake City, Utah | hpc matters.

How does SCC work?

- 12 teams of 6 undergrad. students
  - From all over the world
  - During 3 days at ISC High Performance
- 3 kW power budget
- Several tests
  - HPCC benchmarks
  - 3 full scale apps disclosed in advance
  - 1 “secret” application
  - 1 “secret” challenge
- 3 awards to win
  - Highest HPL
  - 1st, 2nd, 3rd overall places
  - Fan favorite award

And why is this relevant today?

Team 2015

Team 2016

The 2016 team: “Thunderstruck”

- 6 students + 2 advisors from UPC

Dani Filippo Fran Josep Kevin Liz Sandra Ying

- Sponsors

ARM

E4 COMPUTER ENGINEERING

- Academic supporters

UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH
Facultat d’Informàtica de Barcelona

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MONT BLANC

- Industrial supporters

CAVIUM

CoolIT systems

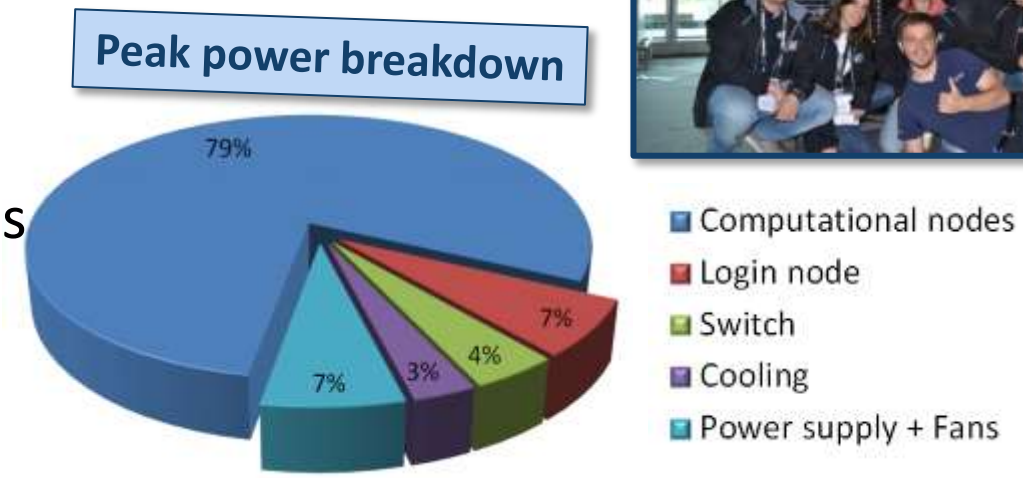
The cluster

Node

- Dual socket motherboard
- Based on 2x Cavium ThunderX SoC
  - 48 cores ARMv8 @ 2.5GHz
- 256 GB DDR4@2.133 GHz
- 240 GB SSD SATA3
- 10/40 GbE interconnect

Cluster configuration

- Liquid cooled
- 1 login node
- 9 computational nodes
- Ubuntu 14.04



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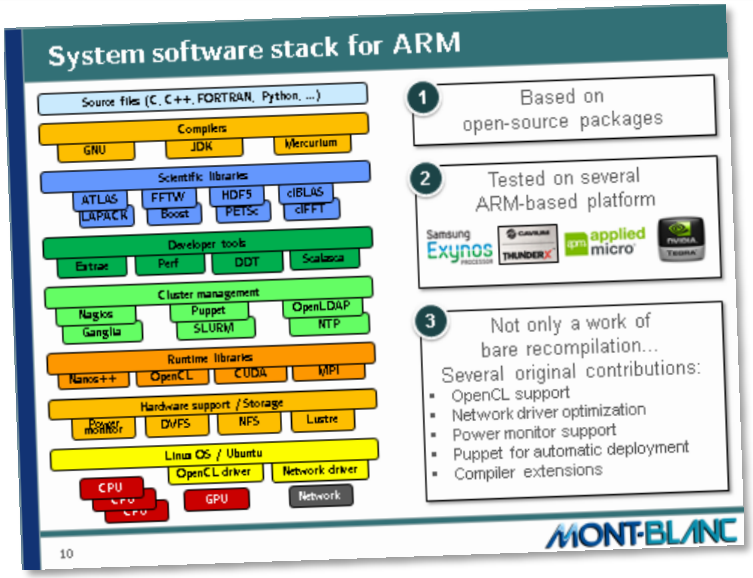
Strategy before the competition



- Main focus on applications
  - Almost no effort in HPCC
- Get the students familiar with
  - How to operate a cluster
  - First run on Mont-Blanc mini-clusters
    - Including power traces
  - Run with realistic input sets
    - Contact application developers for having them
- Interaction with sponsors
  - Almost none with ARM and Cavium
  - High and productive with E4
    - In the attempt of having GPU and Infiniband working
- Analysis using BSC performance analysis tools

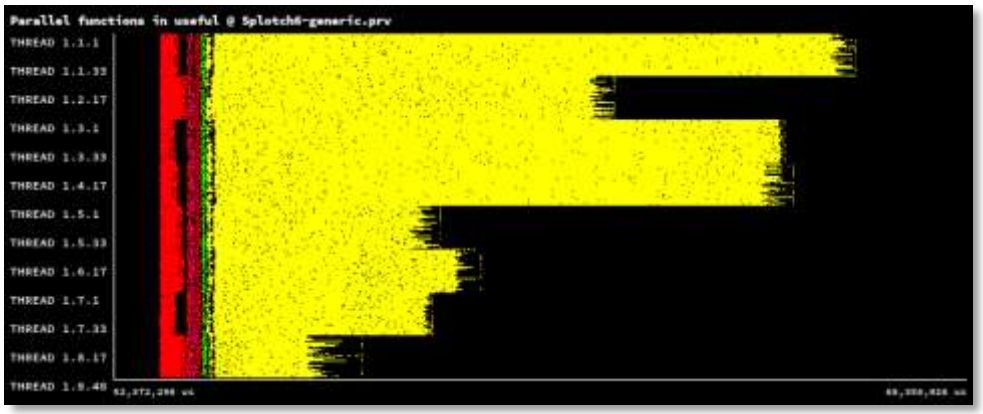
Application performance analysis

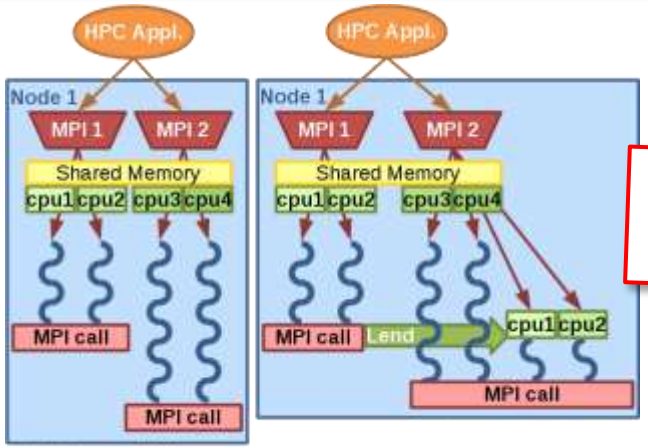
Splotch

- Ray tracer to visualize hydrodynamics simulations
- One of the 2016 applications

Analysis on 4 nodes

- 8 MPI ranks
- 48 OpenMP threads per MPI rank





a) Unbalanced MPI application

b) Unbalanced MPI application balanced with DLB

More info at booth #2511

dynamic load balancing

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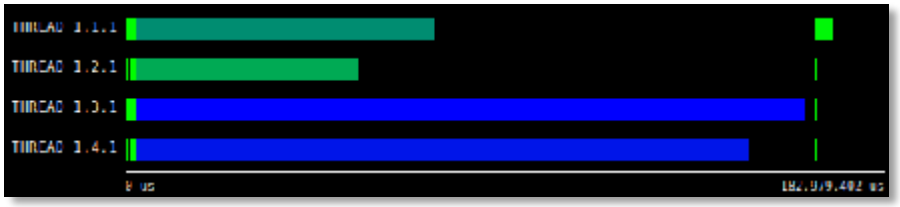
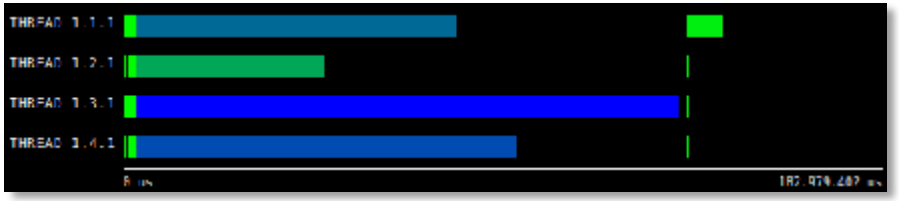
Dynamic Load Balancing in action

- No DLB

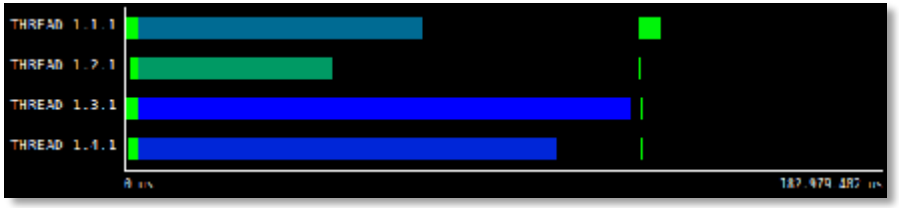


- DLB + Serial mapping

- DLB + Cycling mapping



- DLB + Mapping by-hand



Up to 5x speed up (tuning MPI ranks and OMP threads)!

At the competition…

Day 0	Day 1	Day 2	Day 3
• Setup OK • Hardware reliable	• HPCC • HPL	• WRF • Splotch • Graph500	• Cloverleaf • Secret challenge

- Secret challenge required to re-run two applications so that:
  - They had the lowest peak power possible
  - They finish within one wall clock hour
  - Hardware configuration changes were allowed
- Not much things to do for the secret challenge in our case:
  - No DVFS
  - No GPUs

Lesson learned

- **Students** - Extremely good experience
  - Low level of frustration thanks to maturity of ARM system software
- **Organizers** - Lack of transparency in the evaluation
  - You just know awarded teams
  - If you ask, you get your evaluation, but no ranking nor criteria
- **Sponsors** - The team should interact more with them
  - We realized a bit too late that ARM, E4, Cavium, CoolIT were all extremely collaborative
  - ARM Performance Libraries were there, but we did not use them
    - Still not ready at that time for running a full HPL
  - We would like to have a clear strategy for compilers
    - We rely on gcc, but there is LLVM
    - Cross compiling is not an option
  - Tools for power monitoring!
  - ARM + GPU + IB… Maybe next time!

Contacts

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montblanc-project.eu

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16-17 January 2017

Mont-Blanc event in Barcelona (Spain)

"ARM: On the road to HPC"

http://montblanc-project.eu/press-corner/events/arm-road-hpc

SC06 : Radio Flyer

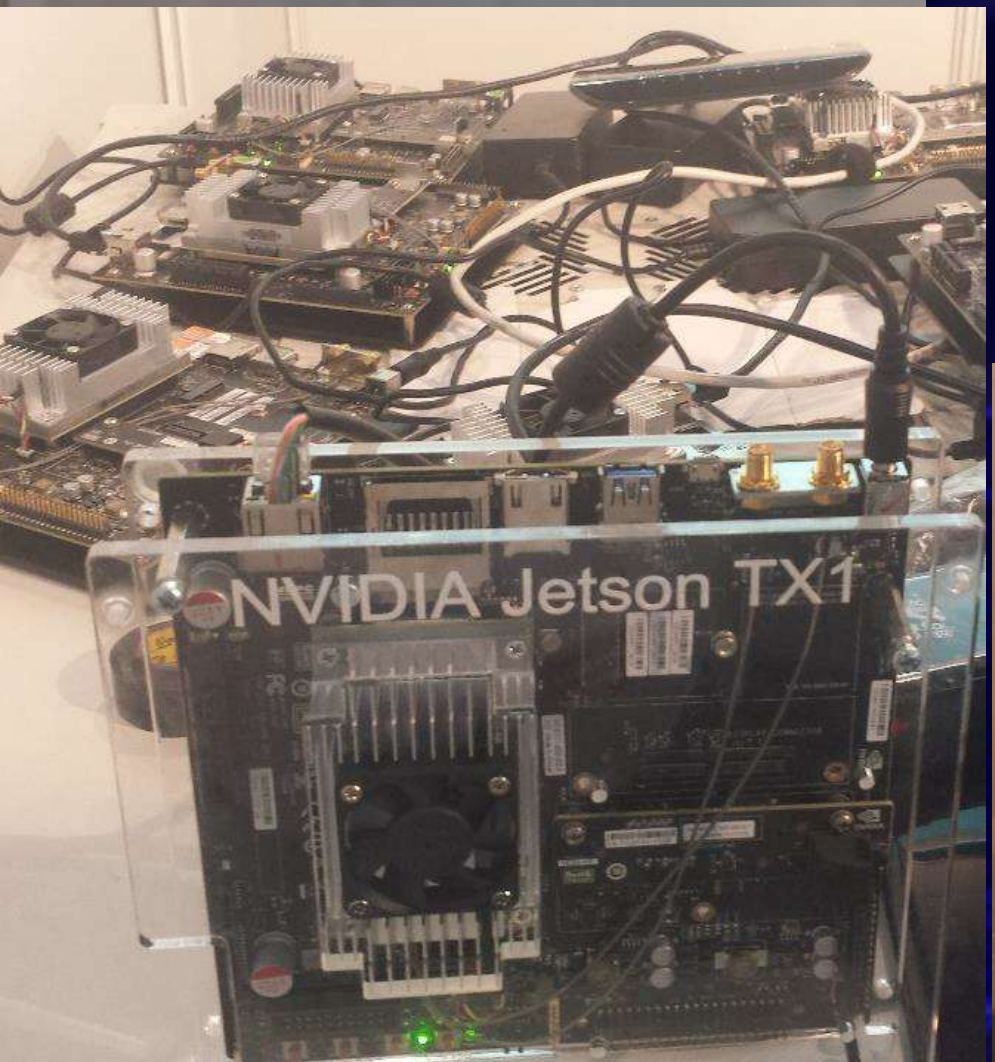
SC07 : Verdex Pro Gumstix

SC10 + Solar powered Supercomputing

SC14 : SoX BoX, NoX Box (ODROID)

SC15 : Nvidia JTK1 Cortex-A15

ISC16 : Ben Nevis JTX1 JetPack 2.2



SC16: Blorenge HyperCube

SC16: omgwiki.org/hpec/files/hpec-challenge/

HPEC17 : Kurze Liste

Performance per Watt per cc

An Investigation of Unified Memory Access Performance in CUDA

Raphael Landaverde, Tiansheng Zhang, Ayse K. Coskun and Martin Herbordt
Electrical and Computer Engineering Department, Boston University, Boston, MA, USA
{soptnrs, tszhang, acoskun, herbordt}@bu.edu

***Abstract*—Managing memory between the CPU and GPU is a major challenge in GPU computing. A programming model, Unified Memory Access (UMA), has been recently introduced by Nvidia to simplify the complexities of memory management while claiming good overall performance. In this paper, we investigate**

and GPU. In particular, we investigate the behavior of UMA memory transfers and analyze whether UMA provides better performance over the standard data transfer implementation as was done prior to the introduction of CUDA 6. We also

Synthetic Aperture Radar imaging on a CUDA-enabled mobile platform

Massimiliano Fatica and Everett Phillips
NVIDIA Corporation
Santa Clara, CA 95050, USA

***Abstract*—This paper presents the details of a Synthetic Aperture Radar (SAR) imaging on the smallest CUDA-capable platform available, the Jetson TK1. The results indicate that GPU accelerated embedded platforms have considerable potential for this type of workload and in conjunction with low power**

memory and a Gigabit Ethernet port plus other peripheral ports (GPIO, mini PCI-e, HDMI, serial, USB). The board consumes 2.2W when idle, around 4-5W when using the CPU cores and up to 11W when using the GPU cores. It uses a Linux

Energy Efficient HPC
Chair: Kurt Keville / MIT ISN, USA

Panel: The Future of Interconnects - Embedded and Big Data
Chair: Craig Lund / Local Knowledge, USA

Panelists:
Bill Boas of System Fabric Works and the OpenFabrics Alliance (RoCE)
Sam Fuller, executive director of the RapidIO Trade Association
Jeremy Kepner of Lincoln Labs and the MIT Big Data initiative
Kurt Keville, Researcher, MIT Institute for Soldier Nanotechnologies
Kalpesh Sheth, Director of Engineering at DRS Intelligence, Communications and Avionics Solu

HPEC Standards BoF
Chair: Hahn Kim / MIT Lincoln Laboratory, USA

Energy Efficient HPC
Chair: Kurt Keville / MIT ISN, USA

IEEE Advancing Technology for Humanity

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Twentieth Annual HPEC Conference
13 - 15 September 2016
Westin Hotel, Waltham, MA USA

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Keynote

- Mr. David Martinez (HPEC Founder, IEEE Fellow; MIT Lincoln Laboratory Associate Head Cyber Security & Information Sciences Division) - *HPEC: The Past, Present and Future Outlook*

Invited Speakers

- Prof. Gilbert Strang (National Academy of Sciences; SIAM Fellow; MIT Mathematics Department) - *Finding the Important Part of a Matrix or Graph*
- Mr. Trung Tran (DARPA MTO - Program Manager) - *Machine Learning, Data Analytics, and Non-Conventional Computer Architecture*
- Mr. Robert Bond (MIT Lincoln Laboratory Associate Head ISR Systems & Technology Division) - *Future DoD Computing and the Emergence of Autonomous Systems*
- Prof. Aleksander Madry (MIT Computer Science & AI Laboratory) - *Linear-Algebraic Methods in Algorithmic Graph Theory*
- Prof. Orran Krieger (Boston University Cloud Computing Initiative) - *The Massachusetts Open Cloud: Vision and Early Experiences*
- Prof. Martin Herbordt (Boston University Electrical & Computer Engineering Department) - *Novo-G#: Large-Scale Reconfigurable Computing with Direct and Programmable Interconnects*
- Prof. Viktor Prasanna (USC Charles Lee Powell Chair in Engineering) - TBD
- Dr. Robert Cunningham (Chair IEEE Cybersecurity Initiative; MIT Lincoln Laboratory Group Leader Secure Resilient Systems & Technology) - *End-to-End Security in the Cloud*
- Dr. Igor Linkov (U.S. Army Corps of Engineers) - *Cyber/Physical Resilience*
- Mr. Clair Grant (Director of R&D VMS Software, Inc) - OpenVMS: *40 Years of Mission*

What's New

Download Call for Papers

Submit to talk or poster presentation

Submit a demo

Important Dates:
Submission Deadline: May 27 2016
Notice of Acceptance: June 17, 2016