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Development of the Post-K Supercomputer

November 14th, 2016
Updated on Nov. 18th

Toshiyuki Shimizu
Vice president, System development division,
Next generation technical computing unit

Post-K is under development, information in these slides is subject to change without notice

FUJITSU HPC and Post-K Development

FUJITSU

- Performance of high-end machines preceding the Post-K
- Post-K
  - Goals and approaches
  - Post-K hardware
  - Post-K software, compilers and their performance
- Summary

Achievements with the K computer

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- Prestigious Benchmark Awards
  - TOP500: 10.5Pflops, 93% efficiency
  - HPCG: 602Tflops, 5.3% efficiency — No. 1
  - Graph500: 38.6TTEPS — No. 1
  - HPC Challenge Class 1: No.1 at all categories — No. 1
    (1) Global HPL, (2) Global RandomAccess, (3) EP STREAM, (4) Global FFT

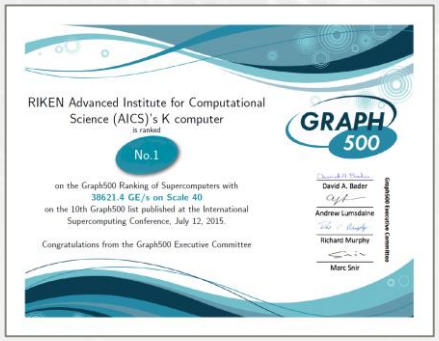
Updated on Nov. 18

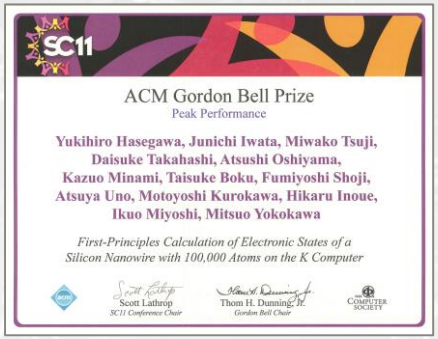
at SC16

6 years from the shipment

- Gordon Bell Prize Awards
  - "First principles calculation of electronic states of a silico nanowire with 100,000 atoms on the K computer" (2011)
  - "4.45 Pflops Astrophysical N-Body Simulation on K Computer – The Gravitational Trillion-Body Problem" (2012)
  - "Simulations of Below-Ground Dynamics of Fungi: 1.184 Pflops Attained by Automated Generation and Autotuning of Temporal Blocking Codes" (2016 finalist)

Nominated as finalist





Post-K Goals and Approaches

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- Goals
  - High application performance and good power efficiency
  - Keeping application compatibility while advancing from predecessors
  - Good usability and better accessibility for users
- Approaches
  - Developing high performance and scalable, custom CPU cores

    【Performance】 Wider SIMD & high memory BW, mathematical acc. primitives

    【Scalability】 SMaC (scalable many core), zero OS jitter (assistant core)

    【Power efficiency】 The best device tech, power control functions, optimal resources
  - Maintaining performance balance and supporting advanced features
    - High memory BW, “Tofu” interconnect, and RIKEN advanced system software
  - Adopting ARM standard architecture
    - Co-operation with ARM/Linux community and utilization of open source software
    - Getting involved in the ARM HPC ecosystem

Post-K Powered by FUJITSU-designed CPU Cores & Tofu

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- FUJITSU CPU cores support ARM SVE ISA
  - FUJITSU, as a lead partner in ARM SVE development, contributes to specification of ARM SVE (Scalable Vector Extension), for application performance
  - FUJITSU ARM core incorporates FUJITSU's proven supercomputer microarchitecture
- ARM SVE, plus optional functions and Tofu, maintain programing models and performance balance
- Post-K complies ARM's standard frameworks (SBSA, etc.), for compatibility among platforms

	Functions for Perf.	Post-K	FX100	FX10	K computer
SVE incorporated	SIMD	512bit	256bit	128bit	128bit
	FMA4	✔	✔	✔	✔
	Math. acc. prim.*	✔Enhanced	✔	✔	✔
Optional functions	Inter-core barrier	✔	✔	✔	✔
	Sector cache	✔Enhanced	✔	✔	✔
	Prefetch modes	✔Enhanced	✔	✔	✔
Interconnect	Tofu	✔Enhanced	✔	✔	✔

*Mathematical acceleration primitives include trigonometric functions, sine & cosines, and exponential…

System Software for Post-K

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- Currently in development, based on "co-design" scheme with application developers, including system hardware

Post-K Applications

FUJITSU Technical Computing Suite / RIKEN Advanced System Software

Management Software	Hierarchical File I/O Software	Programming Environment
System management for highly available & power saving operation	**Application-oriented file I/O middleware**	**XcalableMP**
Job management for higher system utilization & power efficiency	Lustre-based distributed file system FEFS	MPI (Open MPI, MPICH)
		OpenMP, COARRAY, Math Libs.
		Compilers (C, C++, Fortran)
		Debugging and tuning tools

Linux OS / McKernel (Lightweight Kernel)

Post-K System Hardware

FUJITSU Compiler for Post-K

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- Maximizes the execution performance of HPC applications
  - Covers a wide range of applications, including integer calculations are dominant
- Targets 512bit-wide vectorization as well as Vector-length-agnostic
  - Fixed-vector-length facilitates optimizations such as constant folding
- Inherits options/features of K computer, PRIMEHPC FX10 and FX100
- Language Standard Support
  - Fully supported : Fortran 2008, C11, C++14, OpenMP 4.5
  - Partially supported : Fortran 2015, C++1z, OpenMP 5.0
- Supports ARM C Language Extensions (ACLE) for SVE
  - ACLE allow programmers to use SVE instructions as C intrinsic functions

// C intrinsics in ACLE for SVE

```
svfloat64_t z0 = svld1_f64(p0, &x[i]);
svfloat64_t z1 = svld1_f64(p0, &y[i]);
svfloat64_t z2 = svadd_f64_x(p0, z0, z1);
svst1_f64(p0, &z[i], z2);
```

// SVE assembler

```
ld1d    z1.d, p0/z, [x19, x3, lsl #3]
ld1d    z0.d, p0/z, [x20, x3, lsl #3]
fadd    z1.d, p0/m, z1.d, z0.d
st1d    z1.d, p0, [x21, x3, lsl #3]
```

Vectorization by FUJITSU Compiler

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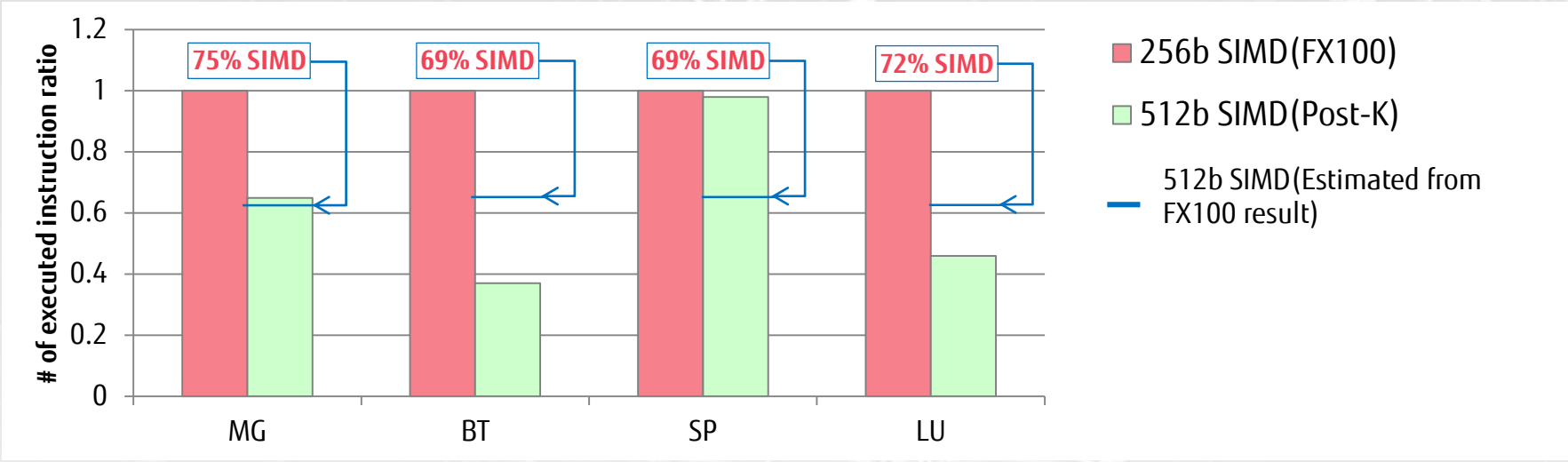
Dynamic instruction counts of representative loops of NPB 3.3-SER



Vectorized loops in TSVC* (Fortran and C)

TSVC	FX100	Post-K
Fortran (135)	96	111
C (151)	106	121

```
// Sample of vectorized loop by SVE
// s482
for (int i = 0; i < LEN; i++) {
  a[i] += b[i] * c[i];
  if (c[i] > b[i]) break;
}
```

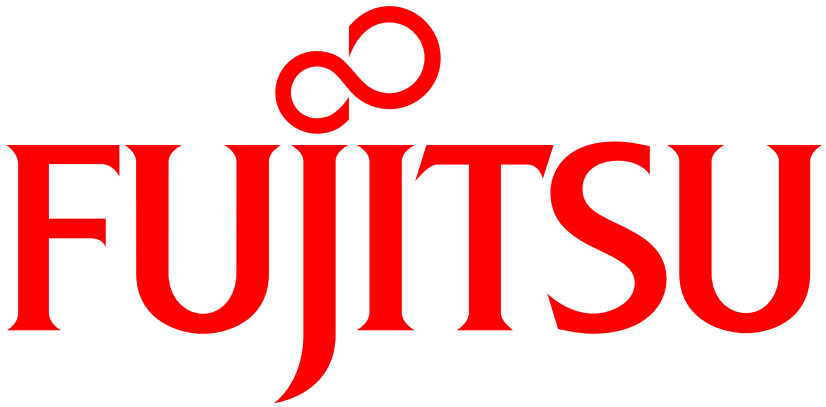
*[Fortran] D. Callahan, J. Dongarra, and D. Levine. "Vectorizing compilers: a test suite and results." In Supercomputing '88, pp. 98- 105.
[C] S. Maleki, Y. Gao, M. J. Garzar´n, T. Wong, and D. A. Padua, "An Evaluation of Vectorizing Compilers," PACT2011, pp. 372-382.

Summary of Post-K Development

FUJITSU

- Developing high performance, scalable, custom CPU cores
  - SMaC architecture with an assistant core for scalable performance
  - ARM instruction set architecture, SVE, as a standard architecture
  - ARM standard frameworks, SBSA, etc., for compatibility among platforms
- Keeping performance balanced and advancing preceding machines
  - Higher performance and higher data bandwidth
- Advanced system software and applications
  - Co-design scheme with application developers
  - FUJITSU optimizing compilers for Post-K

Post-K will meet requirements & be valuable for science and industries



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