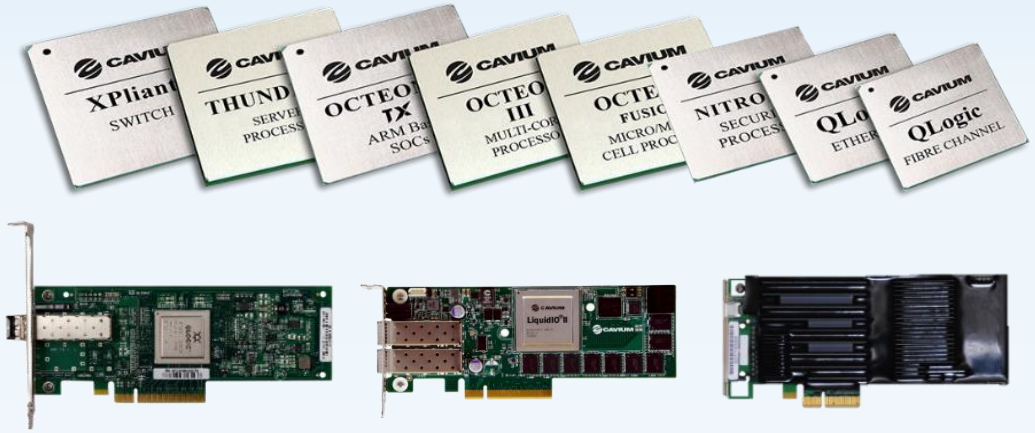
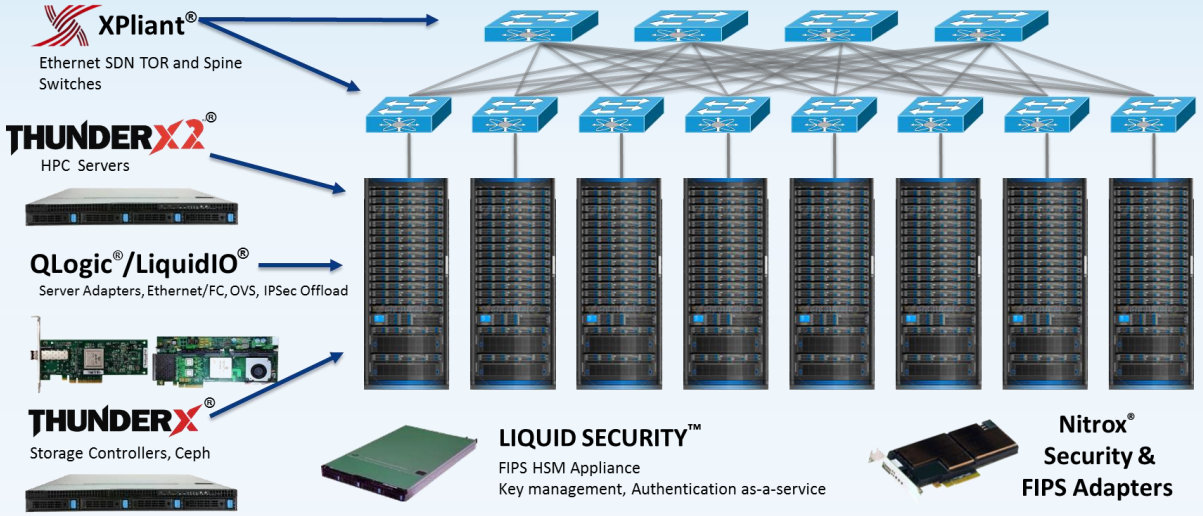
Innovative Alternate Architecture for Exascale Computing

Surya Hotha
Director, Product Marketing

Cavium Corporate Overview





Enterprise | **Mobile Infrastructure** | **Data Center and Cloud** | **Service Provider Cloud**

Multi-Core MIPS, ARM Processors, Security, SDN Switch and Server/Storage Connectivity ~$10B TAM

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Arm & Cavium Enabling Alternate Architecture for HPC

arm	• Most widely used CPU architecture – out ships x86 by 20X • Viable alternative for x86 • Broad ecosystem • Provides optimized compilers, tool chains & libraries for HPC
CAVIUM	• The processor company for the infrastructure • 16+ years of high perf multi core SoC development expertise ARM architecture licensee, broad portfolio of IP • Established leadership in Arm server space: Two generations of custom Armv8-A dual socket server SoC, Xeon E5 class perf

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Key Press at SC17 for THUNDERX2™

"HPE Helps Businesses Capitalize on High Performance Computing and Artificial Intelligence Applications with New High-Density Compute and Storage"

"Cray Catapults Arm-Based Processors Into Supercomputing"

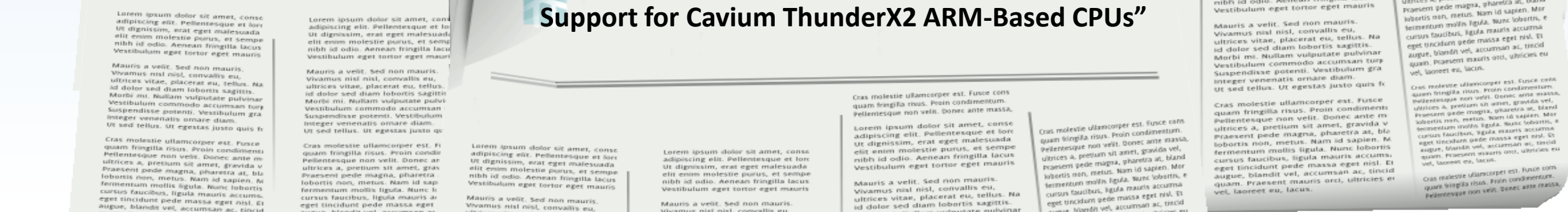
"GIGABYTE Announces Production Availability of Cavium's ThunderX2-based Server Portfolio"

"Ingrasys Announces Production Systems Based on Cavium's ThunderX2 Processor"

"ARM Benchmarks Show HPC Ripe for Processor Shakeup"

"Red Hat introduces Arm server support for Red Hat Enterprise Linux"

"Microsemi Announces Adaptec Smart Storage Adapter Support for Cavium ThunderX2 ARM-Based CPUs"



Cavium Receives Honors in 2017 HPCwire Readers' and Editors' Choice Awards

- **Best HPC Collaboration (Academia/Government/Industry) -- Editors' Choice**
  - European R&D project Mont-Blanc investigates a new type of energy-efficient computer architecture for HPC, leveraging Cavium's ThunderX2 Arm-based processor

- **Top 5 New Products or Technologies to Watch -- Editors' Choice**
  - Bull Sequana X1310, with Cavium's ThunderX2 Arm-based processor

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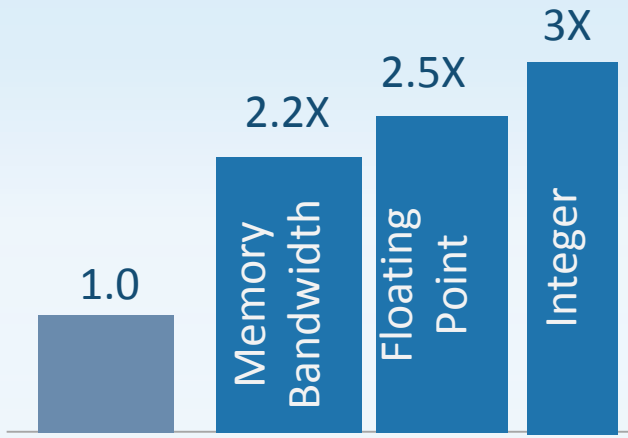
ThunderX Momentum in HPC Continues to Grow…



2-3X better HPC performance

Server platforms at World's premier HPC Labs

Significant HPC Engagements

OEM Partners

Hewlett Packard Enterprise

HPE Apollo 70

2U Industry Standard Form Factor using HPEs scalable HPC enclosure.

1U Tray for highest compute density (4x 2P Nodes per Enclosure)

2U Tray for addition of acceleration (2x 2P + 2GPU Nodes Per Enclosure)

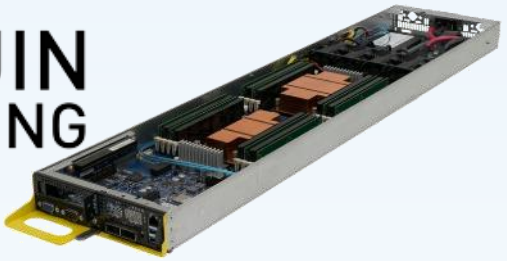
Hot pluggable trays, HPE Gen-10 Power supplies.
Reliable and proven infrastructure.

Atos

X1310- Bull Sequana Compute Blade

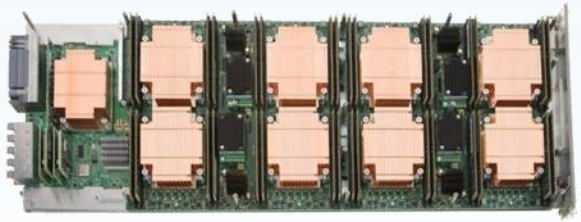
TundraTM Extreme Scale

PENGUIN COMPUTING



CRAY

XC50 Supercomputer



- Chassis with 16 compute blades
- 128 Sockets
- Inter-Aries communication over backplane

Hot pluggable trays, 4x 2P Nodes per blade

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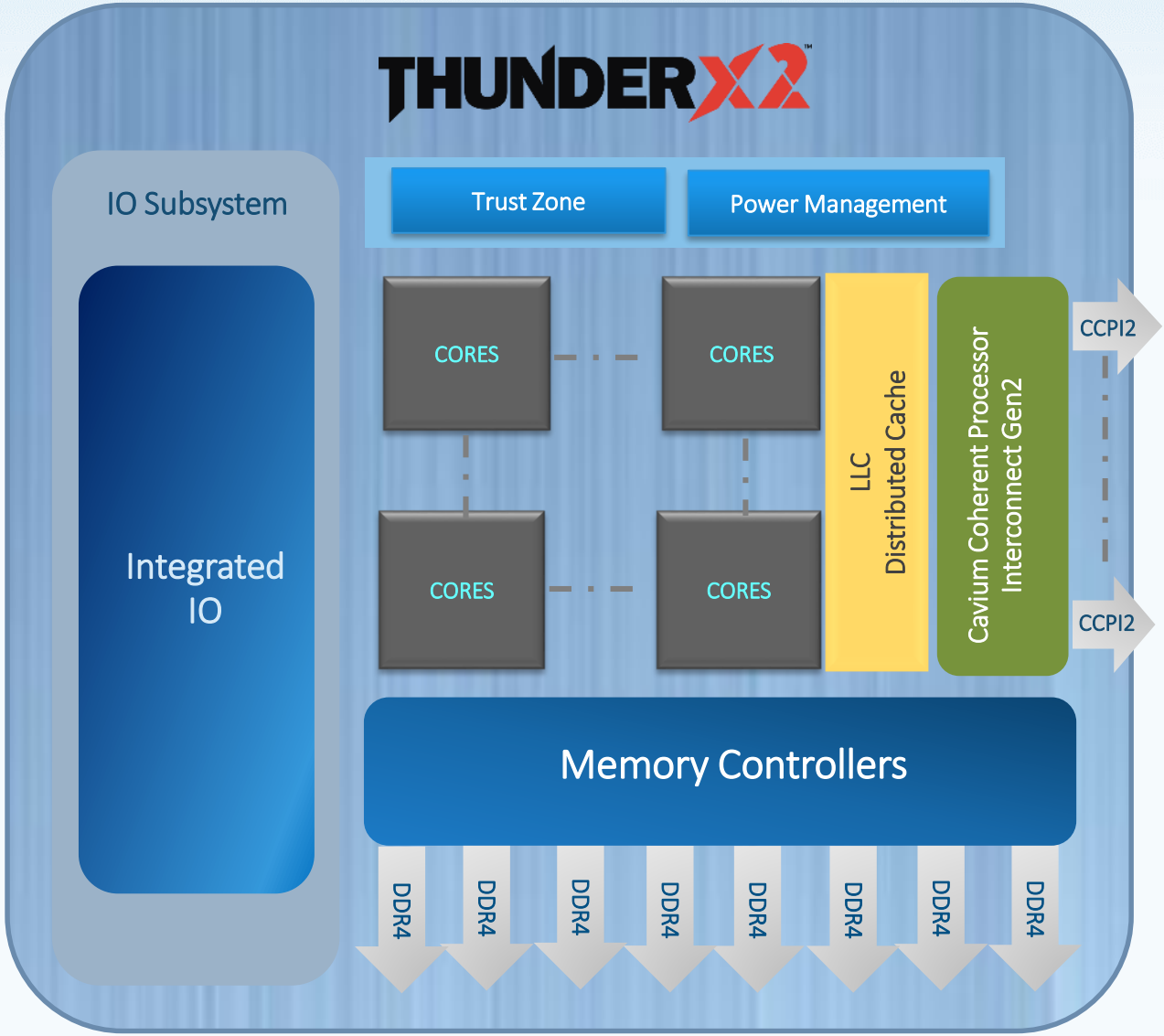
Cavium CN99XX - 1st member of THUNDERX2 Family



- 24/28/32 Custom ARMv8 cores
- Fully Out-Of-Order (OOO) Execution
- 1S and 2S Configuration
- Up to 8 DDR4 Memory Controllers
- Up to 16 DIMMs per Socket
- Server Class RAS features
- Server class virtualization
- Integrated IOs
- Extensive Power Management

2nd gen Arm server SoC

Delivers 2-3X higher performance

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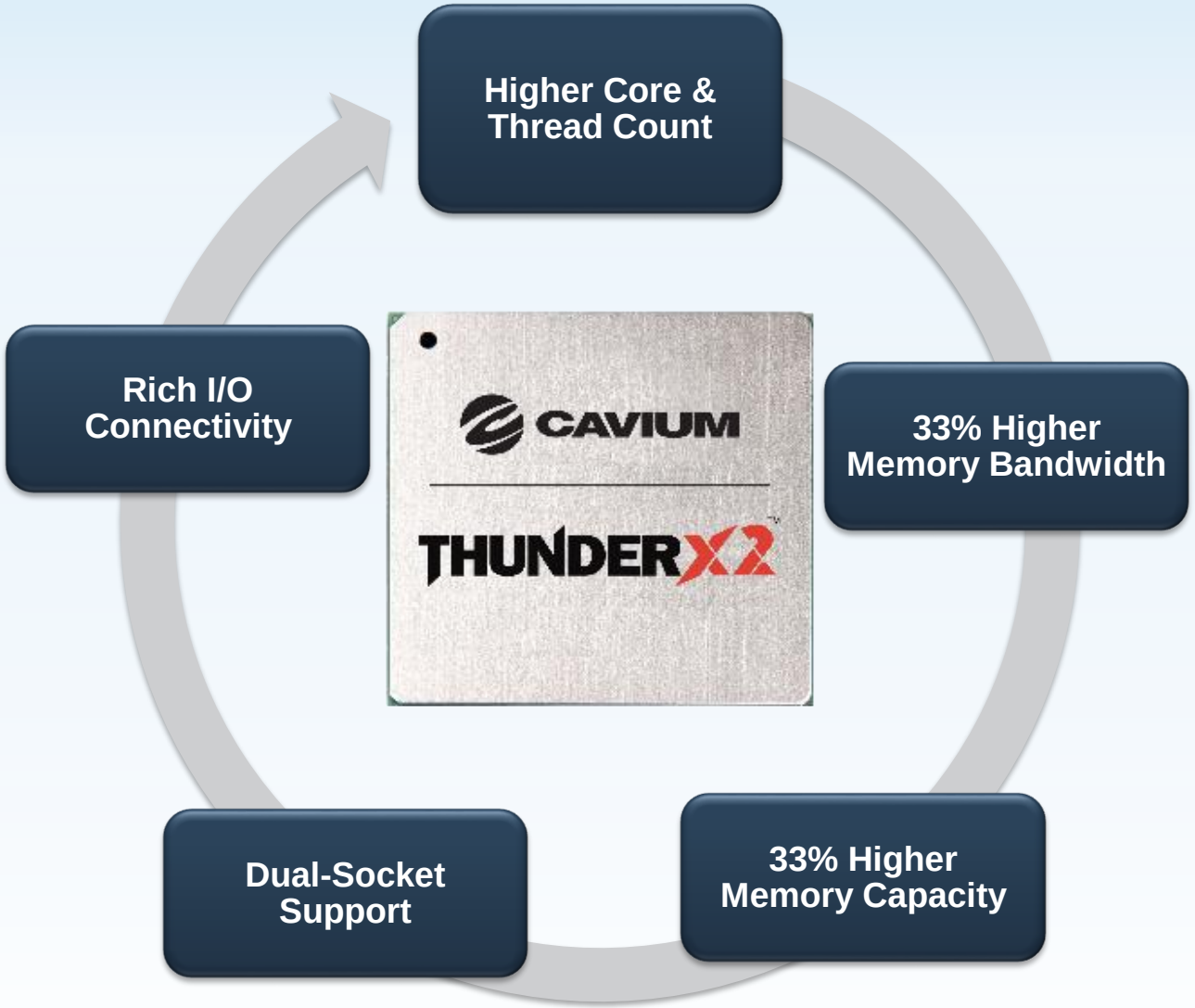
Key Differentiators of THUNDERX2



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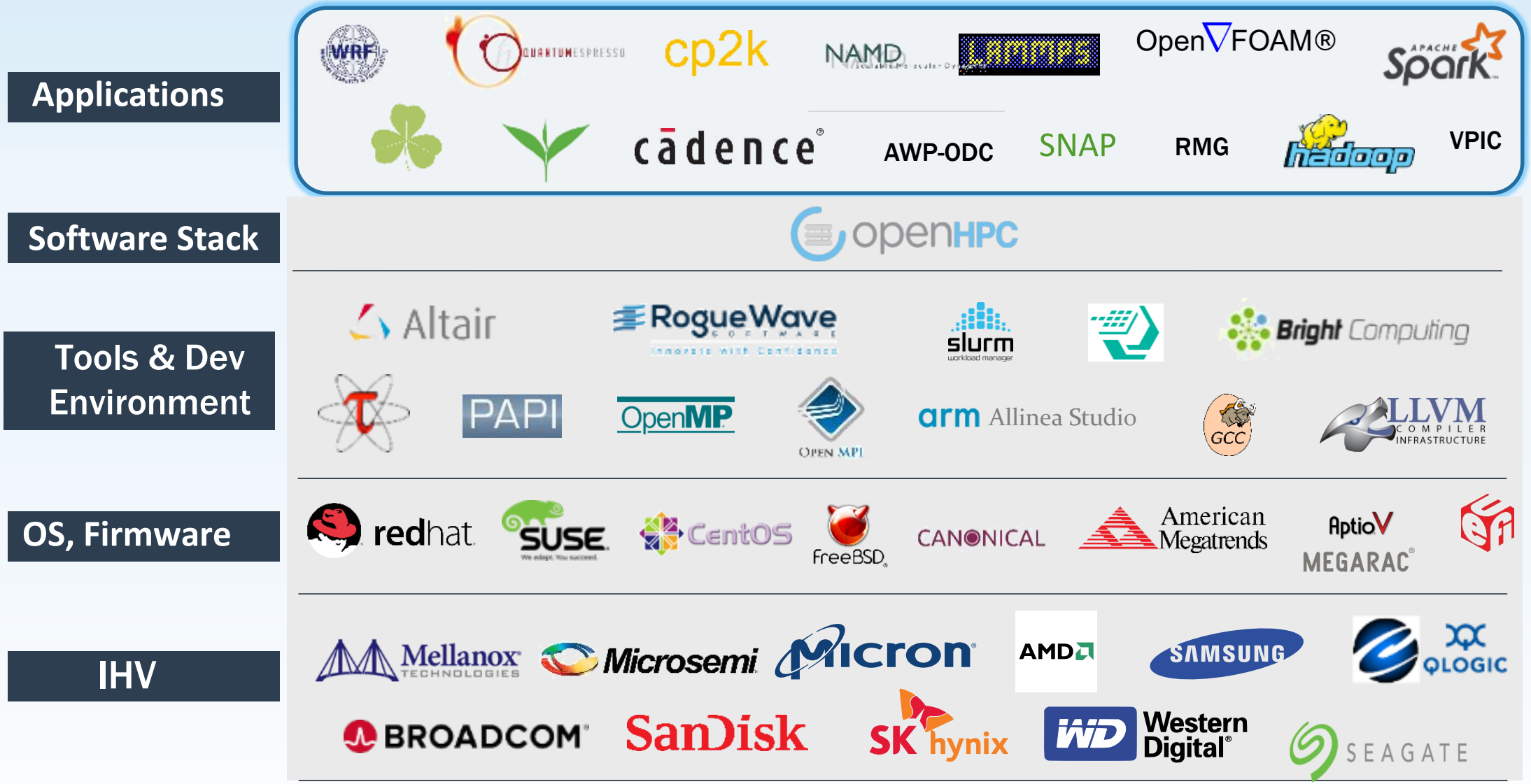
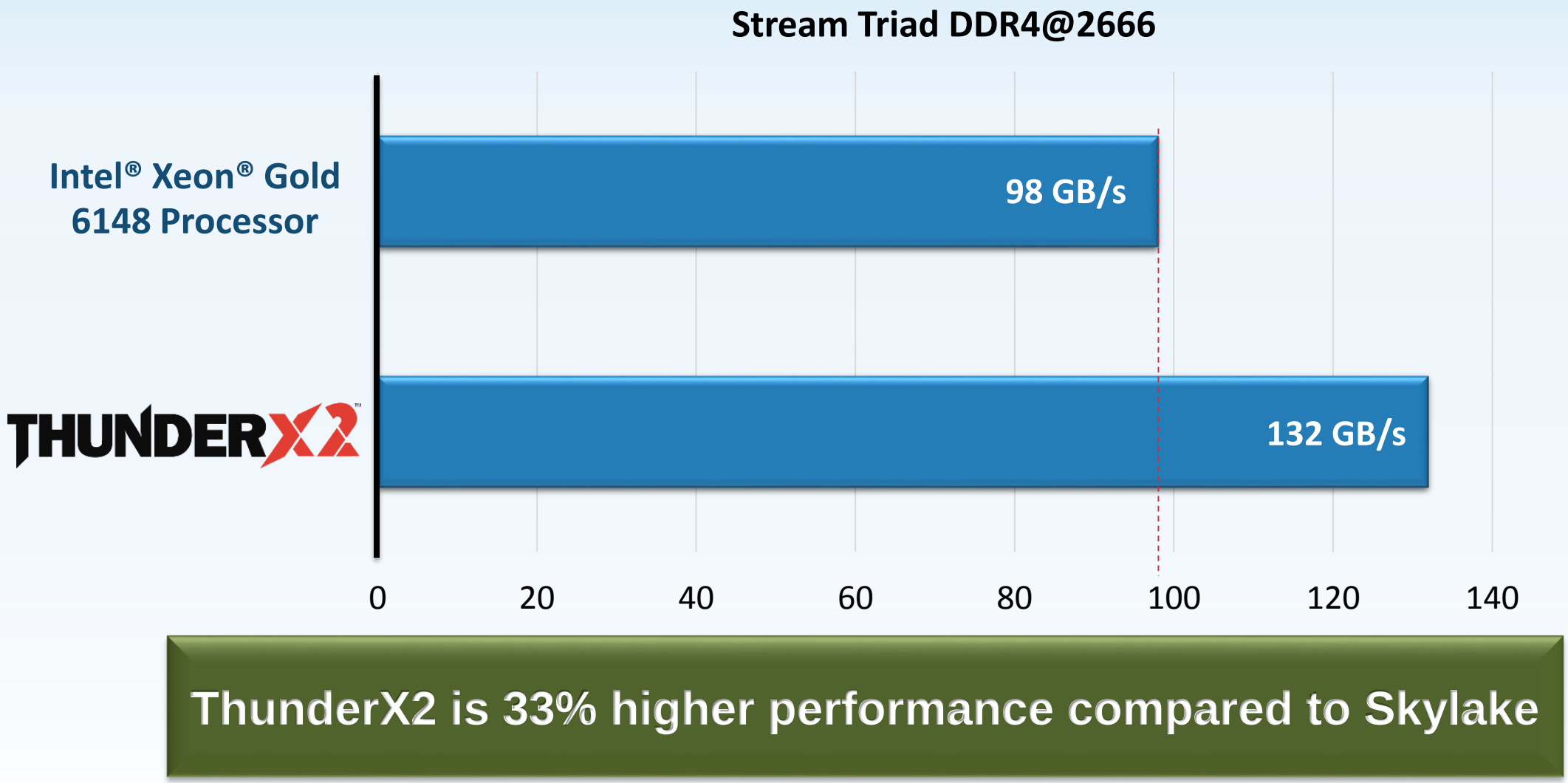
THUNDERX2 Comprehensive HPC Ecosystem



Commercial Compiler, Tool Chain, Libraries available from Arm (Allinea Studio)
Support for community codes rapidly increasing

ThunderX2 Memory Bandwidth



ThunderX2 is 33% higher performance compared to Skylake

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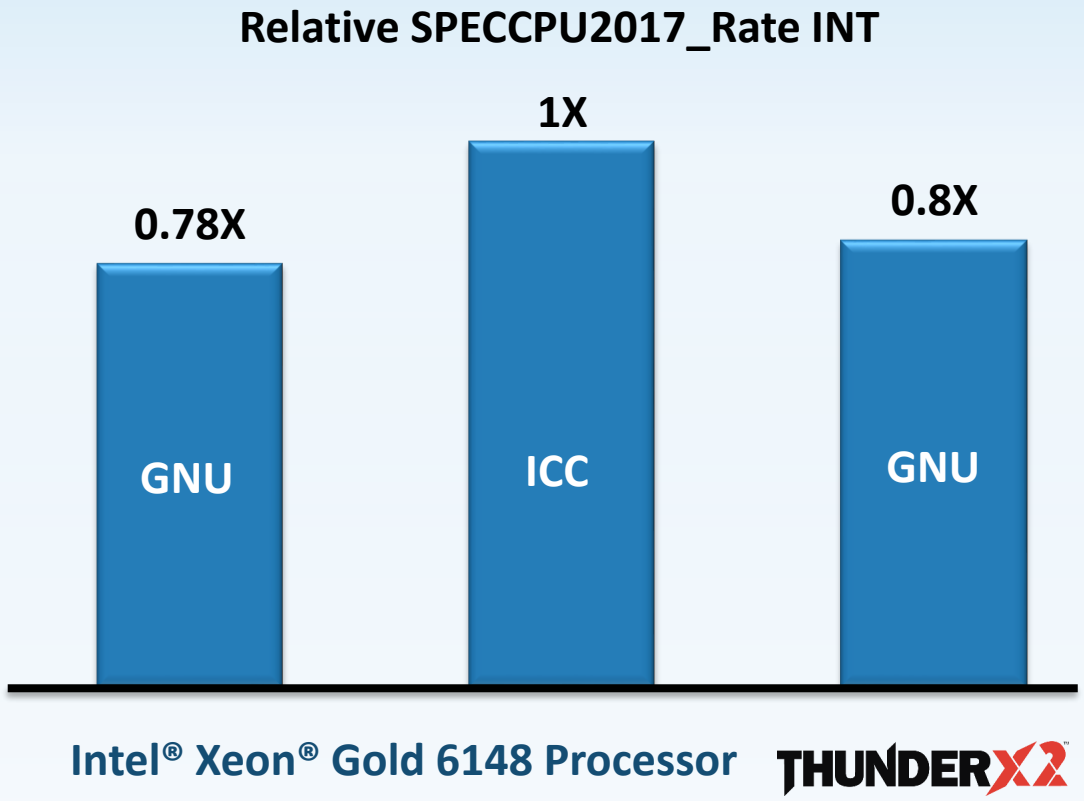
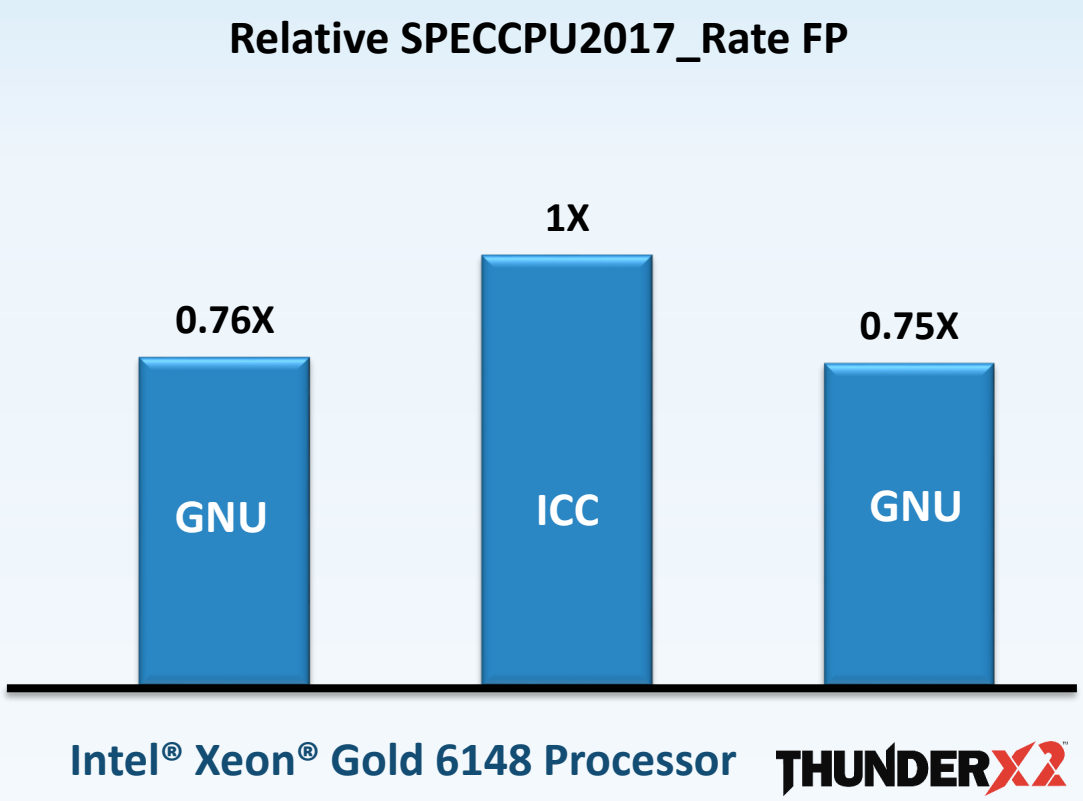
ThunderX2 SPEC CPU® 2017 Rate Performance





Cavium + Arm working on optimized compilers
Target: ~15% higher perf

icc18	-O3 -xHost -ipo -O3 -no-prec-div -auto-P32 -qopt-prefetch -qopt-mem-layout-trans=3
Gcc 7.2	-Ofast -flto -mabi=ilp32

*Measured ThunderX2 perf projected for production silicon w/ Turbo

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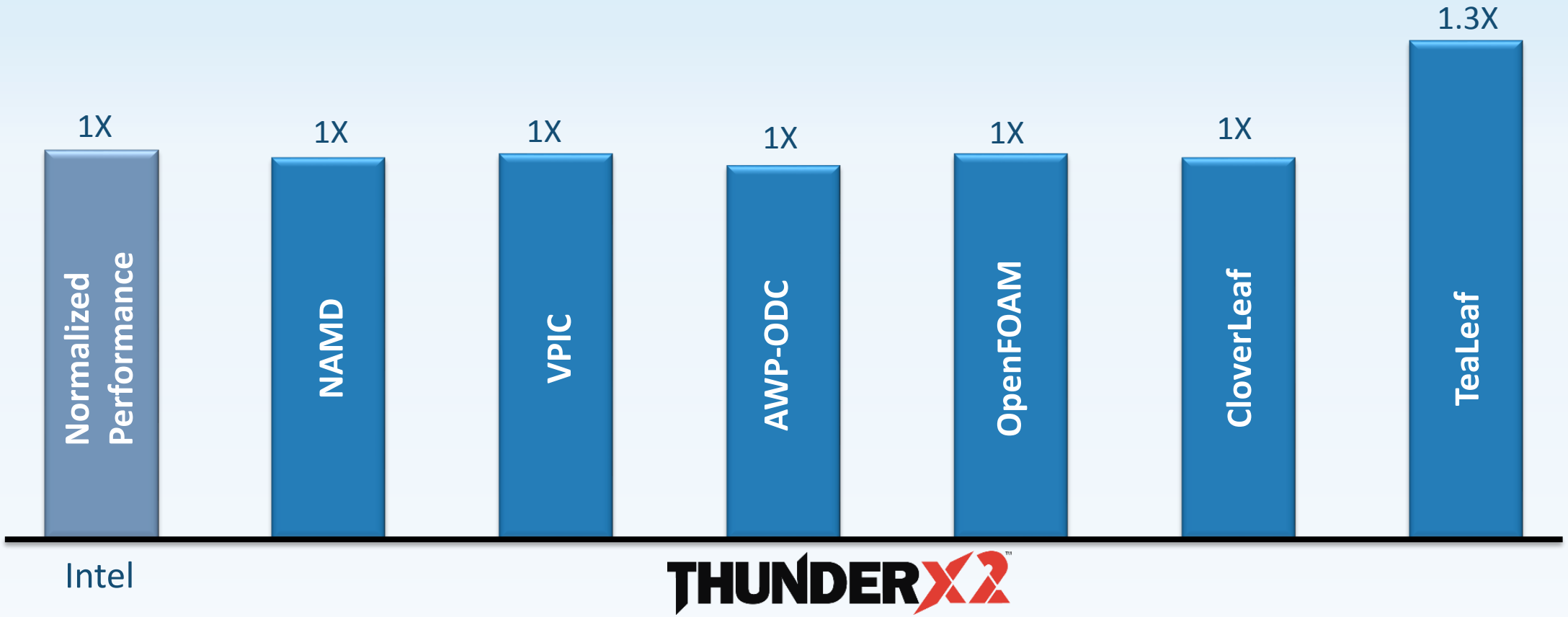
ThunderX2 Performance vs Intel® Xeon® Gold



Cavium ThunderX2: 32 core 2.2GHz using gcc 7.2 and open source libraries (OpenBLAS, FFTW, OpenMPI…)
Intel® Xeon® Gold 6148 Processor: 20 core, 2.4 GHz, with ICC18 and Intel optimized libraries (MKL, IntelMPI, Intel FFTW…)

Cavium + Arm + Partners working on vectorizing compiler & optimized libraries
Target: ~15% higher perf

Cavium at SC17 – Booth#349

Presentation @Arm HPC User Group, *Cavium ThunderX2 – Applications & Performance*

2.30p-2.45p, Monday: *Aspen Ballroom, Grand Hyatt Hotel*

Presentation, *Innovative Alternate Architecture for Exascale*

10.30a-11a, Tuesday: *RedHat mini-Theater*

Presentation @Exhibitor Forum, *Innovative Alternate Architecture for Exascale*

2.30p-3p, Tuesday: *SC Room 501-502*

Presentation @HPE, *Innovative Alternate Architecture for Exascale*

2.30p-3p, Tuesday: *HPE mini-Theater #925*

Partner Panel: *The Arm Software Ecosystem: Are We There Yet?*

1:30-3 pm, Tuesday: *SC room 201-203*

Speakers include: nVidia, CERN, U. Bristol and U. Michigan

BoF : *Arm User Experience: Testbeds and deployment at HPC centers*

5:15 pm, Tuesday: *SC room 701*

Speakers include: Oak Ridge, RIKEN and Bristol

Presentation, *Innovative Alternate Architecture for Exascale*

2.30p-3p, Wednesday: *SUSE booth*

Also look out on the exhibition floor for booths from Cavium partners.

To schedule a private meeting, e-mail: Lilly.Ly@cavium.com

Innovations For Exascale Computing