arm Training

Introduction to the AMBA ACE Protocol

Summary:

This training topic covers essential information on Arm's AMBA ACE protocol. System-level coherency enables the sharing of memory by system components without the software required to perform software cache maintenance to maintain coherency between caches. This course is aimed at anyone designing, verifying, or integrating ACE components into a system.

The course starts by providing a refresher on the underlying AXI protocol before giving an overview of the ACE protocol itself. It looks at the problems associated with delivering system-level coherency and how ACE provides hardware coherency protection.

Next, the course looks at the additional channels and signals that ACE provides to ensure this protection before moving on to look at some different transaction types with examples of coherent operations so you can see how the transactions are ordered.

Over the coming weeks the course will be expanded to cover additional topics such as exclusive accesses, how ACE support barriers, distributed virtual memory (DVM), and the subset of ACE, ACE-Lite.

Prerequisites:

A basic understanding of AXI is recommended.

Audience:

The course is relevant to anyone designing, verifying, or integrating ACE components into a system.

Delivery Method:

Online

Length:

2 hours

Modules:

Introduction

- AMBA's evolution
- AXI review
- AXI features
- No coherency
- Coherency solutions
- Cache line states
- Coherent reads and writes

Channels and signals

- ACE channels
- Additional channel signals
- Shareability domains
- ACE transactions
- Snoop response signaling
- Extra RRESP bits
- RACK and WACK

Transaction flow

- Shareable read - miss
- Shareable read - hit
- Shareable write - write-back caching, full line.
- Shareable write - write-back caching, partial line
- Shareable write - write-through caching
- Two ReadUnique transactions to the same line

Coming soon...

- Exclusives
- Barriers
- ACE-Lite
- DVM transactions