ARM Cortex-A35 MPCore Hardware Design

Summary:

This course is designed for those who are designing hardware based around the Cortex-A35 MPCore processor.

Prerequisites:

- Comprehensive knowledge of the ARMv8-A architecture (see notes below)
- Familiarity with the AMBA on-chip bus architecture
- Knowledge of embedded systems
- Experience with digital logic and hardware/ASIC design issues

Audience:
Hardware design engineers who need to understand the issues involved when designing SoCs around the ARM Cortex-A35 MPCore processor.

Course Length: 3 days

Modules:

- Cortex-A35 Processor Overview
- ARMv8-A Architecture Overview
- Cortex-A35 Processor Core
- Cortex-A35 Memory Management Unit
- Cortex-A35 Memory Sub-Systems
- Cortex-A35 Clocks and Resets
- Cortex-A35 Power Management
- CCI-400 Cache Coherent Interconnect (or CCN-504 Cache Coherent Network)
- GIC-400 Interrupt Controller (or GIC-500 Interrupt Controller)
- Cortex-A35 System Design Considerations
- Cortex-A35 Debug
- Cortex-A35 Booting
- Cortex-A35 Configuration
- Cortex-A35 Integration Summary

Notes:

For students who do not have the pre-requisite knowledge of the ARMv8-A architecture and AMBA, we provide an optional one-day introductory course on these subjects.